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IP67A-AHT REV 5.0

CPU:

Intel Sandy Bridge processors in LGA1155 Package

System Chipset:

Cougar Point

Main Memory:

Dual Channel/DDR-III*4(Max 16GB) 1066/1333

Onboard Device:

Clock Generator:RTM885T-926

Super I/O:ITE8728

LAN:Realtek 8111E

HD Codec:ALC892

IDE/1394 Host controller:VT6315N

PCI BRIDGE:IT8890

Expansion Slots:

PCI EXPRESS 16X SLOT*2

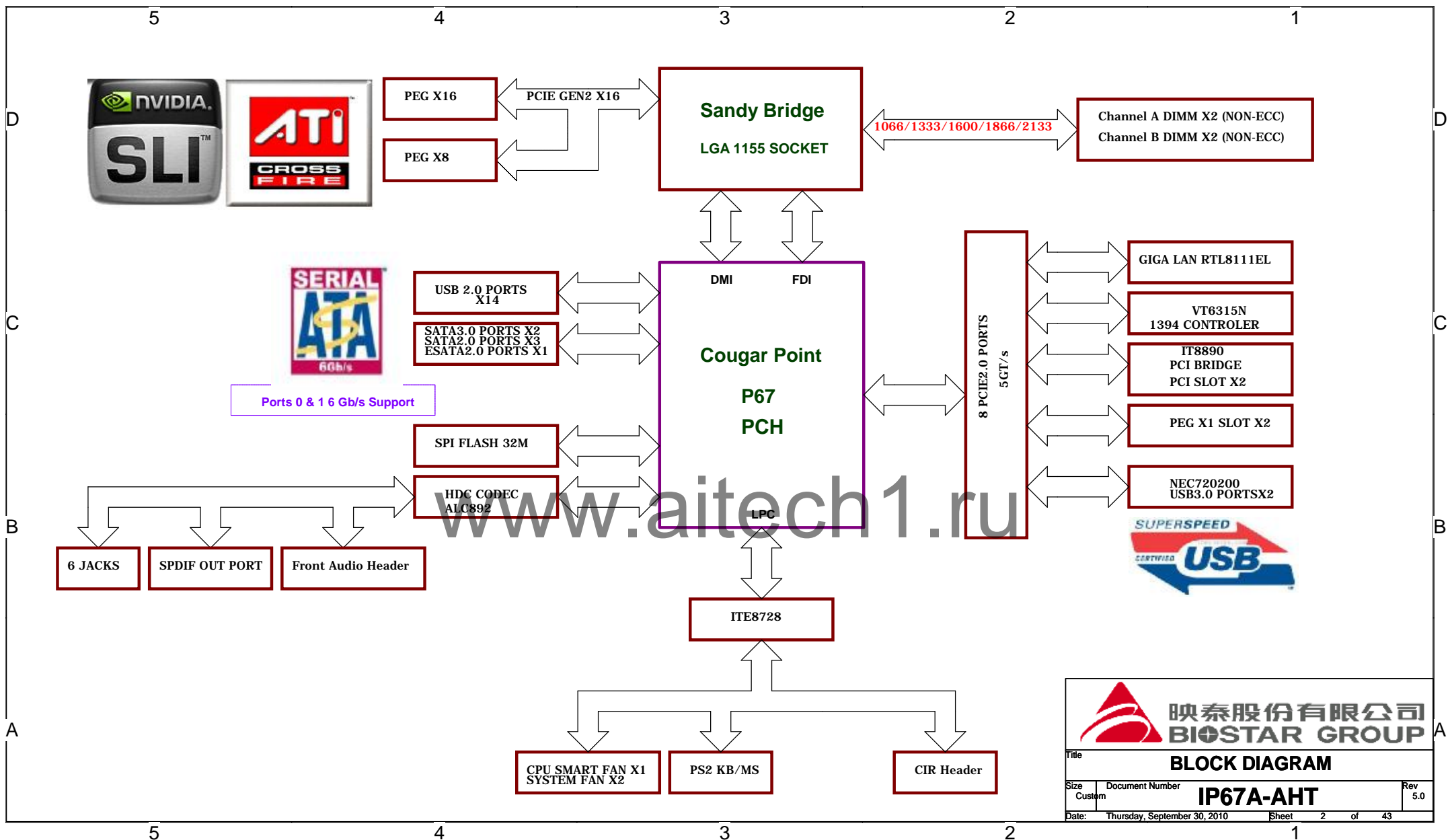
PCI SLOT*2

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Title INDEX			
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5
ver:0.5 to 0.51

1. PCI-E x16 slot: 2(x16+x4) change to (x8+x8) (PAGE.17)
2. Change CLOCKGEN BTM / ICC Mode colay (PAGE.4/13)
3. Change CPU CORE PWMuP6235,6 PHASE to 8 PHASE (PAGE.35/36)
4. Change VTT PWM to uP6219B (PAGE.34)
5. Change RCA +SPDIF connector type(UP RCA LOW SPDIF (PAGE.23)
6. Add USB bluetooth+DUAL USB controller (PAGE.28)
7. Add CPU VCCIO_select for IVY bridge (PAGE.34)
8. Remove CPU DBR# function (PAGE.5)
9. Change USB Legacy PCH GPIO57 to GPIO8 (PAGE.12)
10. Add Thermal Protection and report circuit when entry VR HOT# in TURBO BOOST mode (PAGE.31)
11. Update PCH ORCAD library to V.1.1 (pin A54/A52/F57/D57 change to VSS, remove NVRAM interface, add pin BR54 PCHHOT# (PAGE.10-15)
12. Remove ALL IP05_ME power for NON-AMT platform (PAGE.38)
13. Change SATA Port 1/2 CONN TYPE to right angle (PAGE.11)
14. Remove all PCH PLL LC filters for external graphics design (PAGE.14)
15. Remove SIO IT8728 ATX level shift ,PIN 19 Can use 5V level, didn't level shift and add PCH SM LINK BUS to SIO PIN 120/121 (PAGE.25)
16. Update new IT8893E AX library, change CLOCK and PME circuit (PAGE.19)
17. Change 3V3_Dual and VCC3 switch circuit (PAGE.30)

ver:0.51 to 0.52

1. Change USB bluetooth+DUAL USB CONN to DUAL USB CONN (PAGE.28)
2. Modify Front Panel power LED circuit (PAGE.29)
3. Modify Over voltage LEVEL form 15mv to 1.24~1.27mv (PAGE.32,33)
4. Modify CPU VTT VCCIO_select circuit used VID3 only (PAGE.32,33)

ver:0.52 to 0.55

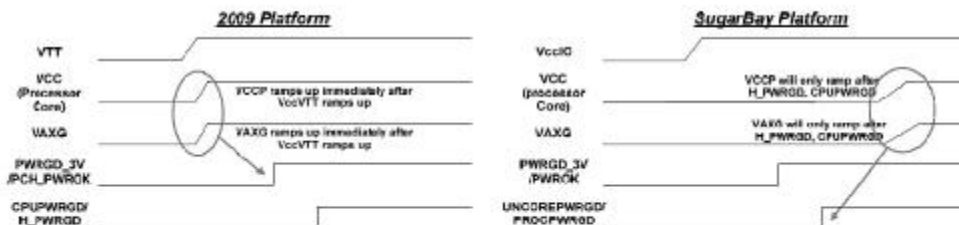
1. Change IT8893E Rev:AX to BX (PAGE.24)
2. Modify USB 3.0 circuit (PAGE.46)
3. Modify 3V_SB power circuit (PAGE.38)
4. Modify HD CODE +5VA decoupling CAP for burn in POP sense issue (PAGE.22)
5. Remove CK505 and change SYSTEM CLOCK form BTM to ICC MODE

ver:0.55 to 5.0

1. Remove "VR_RDY" Pull up resistor to "V_CPU_VCCIO" (PAGE.35)
2. Re-layout SW6&SW2 for current un-balance
3. Remove USB3.0 pin H1 SMIB function (PAGE.42)
4. Adjust LDO power LEVEL to meet standard SPEC (PAGE.32)
5. Add V_SA level select circuit (PAGE.32)
6. Correct Q53 MOSFET package to SOT669 (PAGE.32)

• Changes from 2009 Platform – Sugar Bay:


1. VCCP (Processor Core) and VAXG rails only turn on AFTER the H_PWRGD, CPUPWRGD, and other uncore PWRGD signals assert.
2. Additional DSW state entry/exit power sequence.

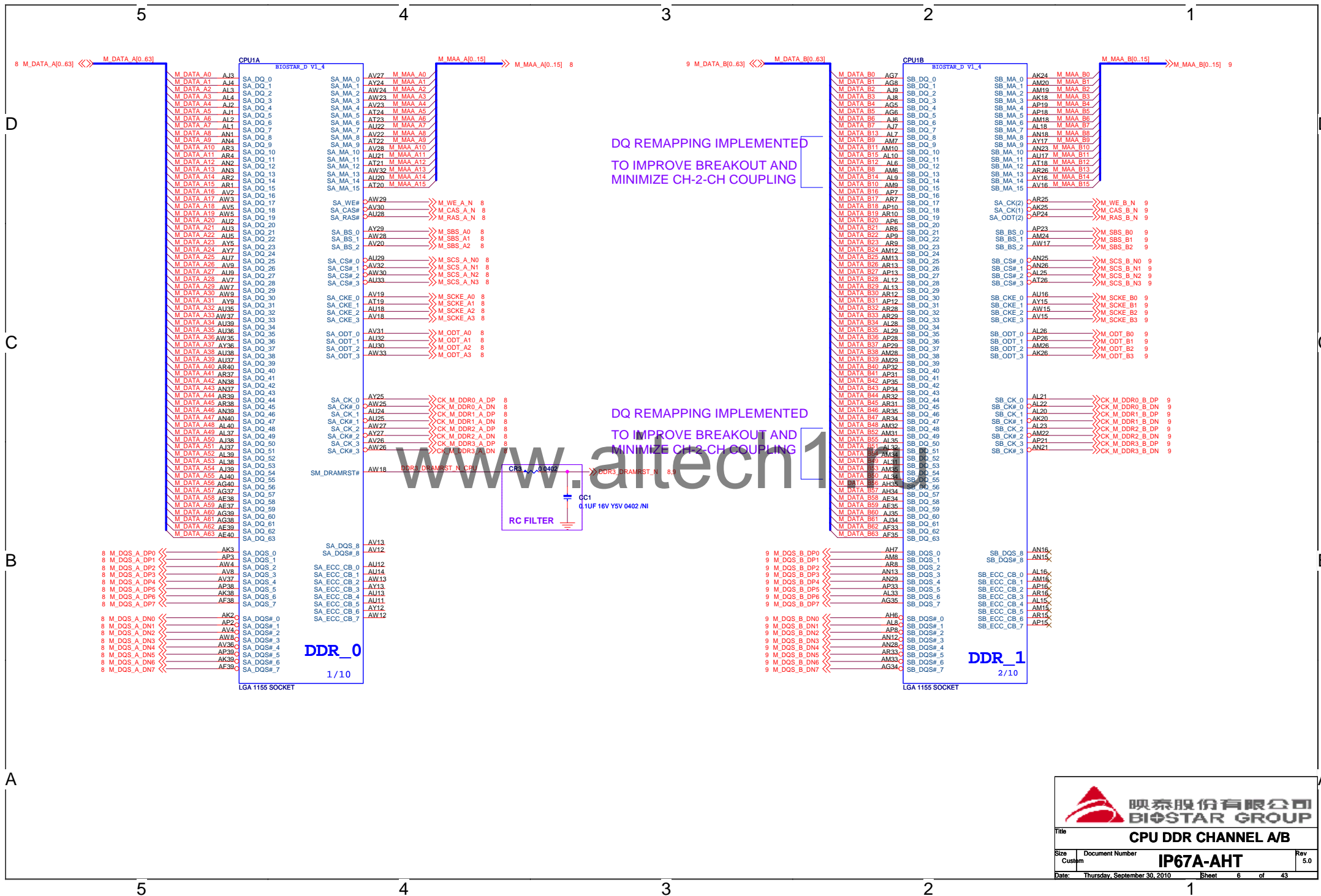


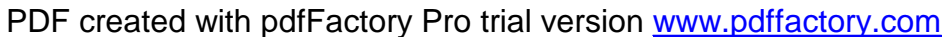
VCCP & VAXG power sequence comparison

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Change List			
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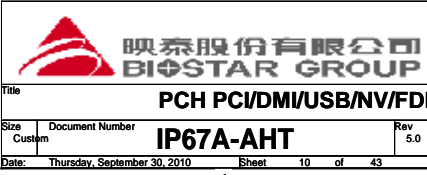
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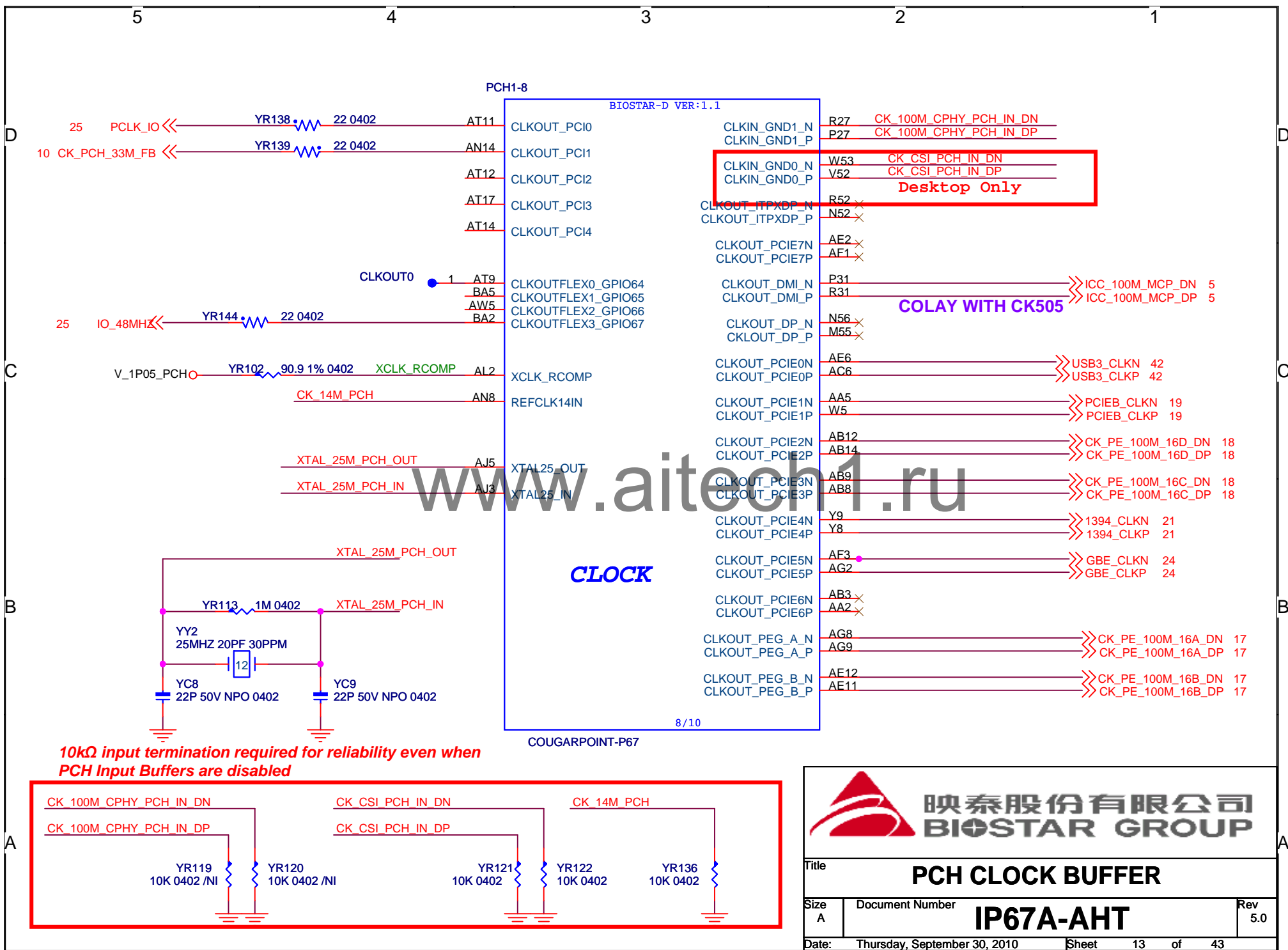
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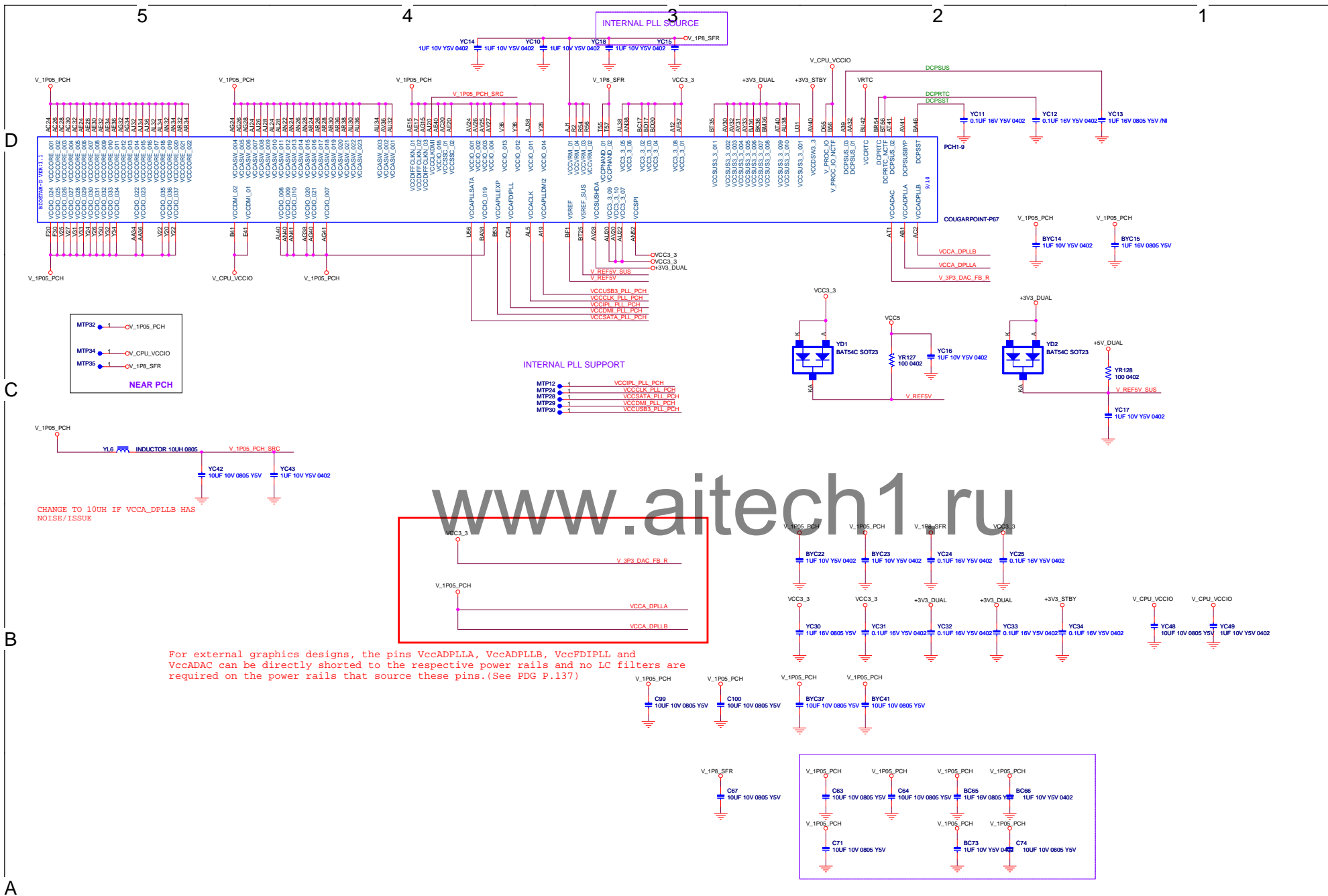




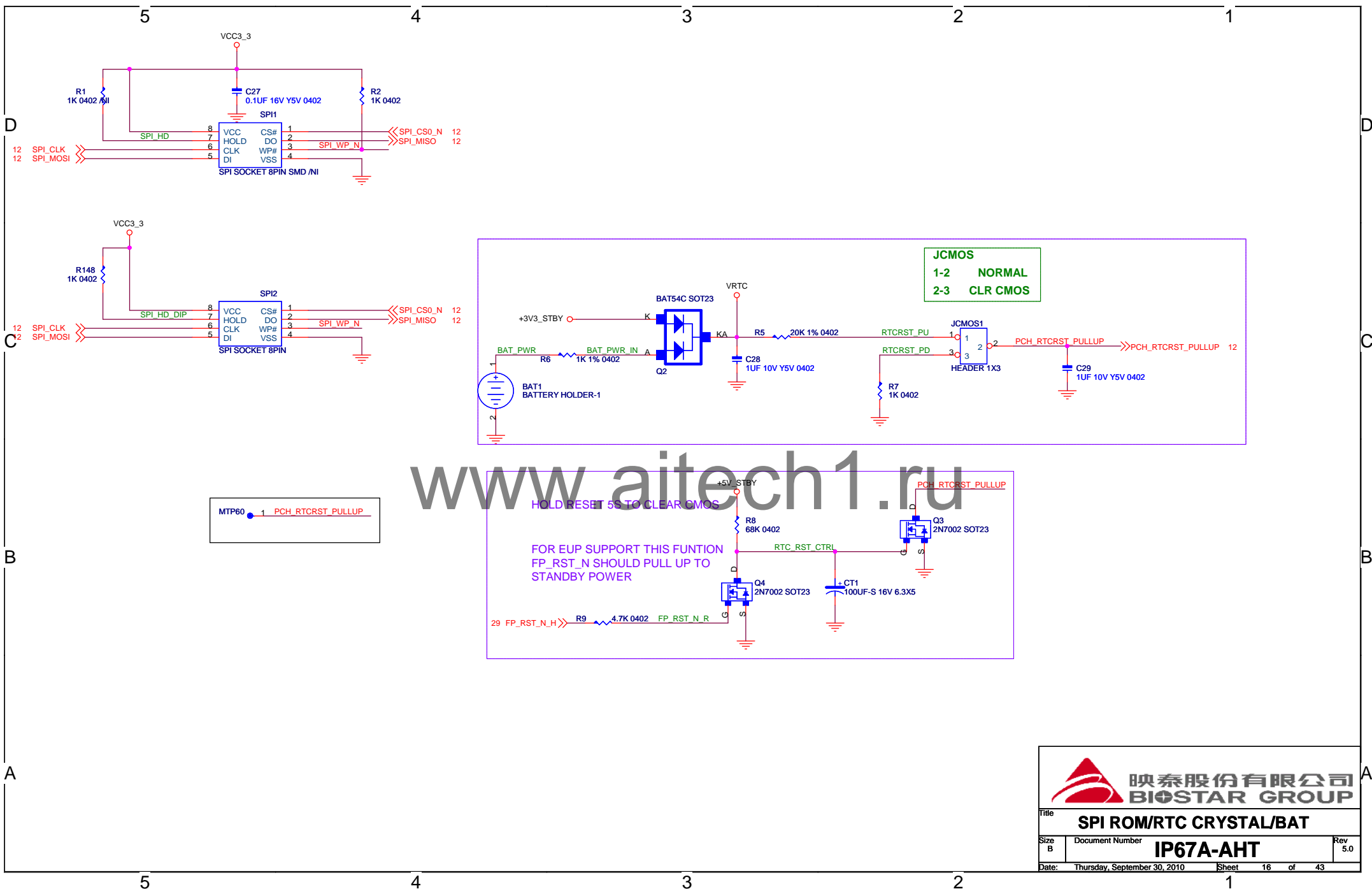


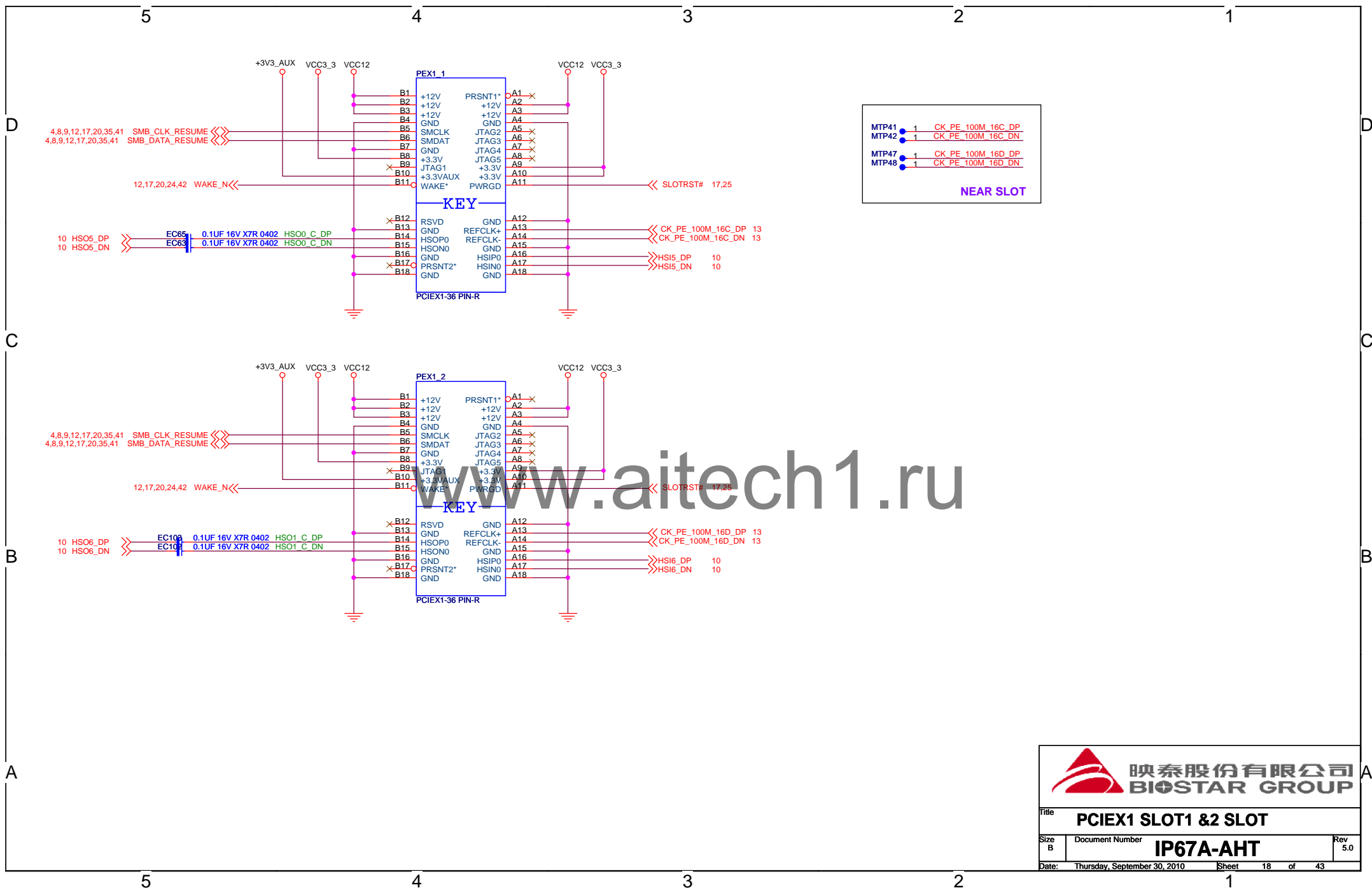




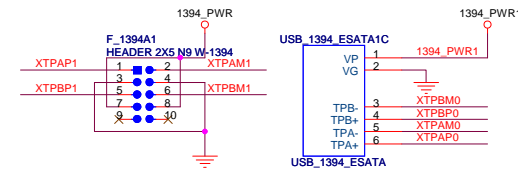
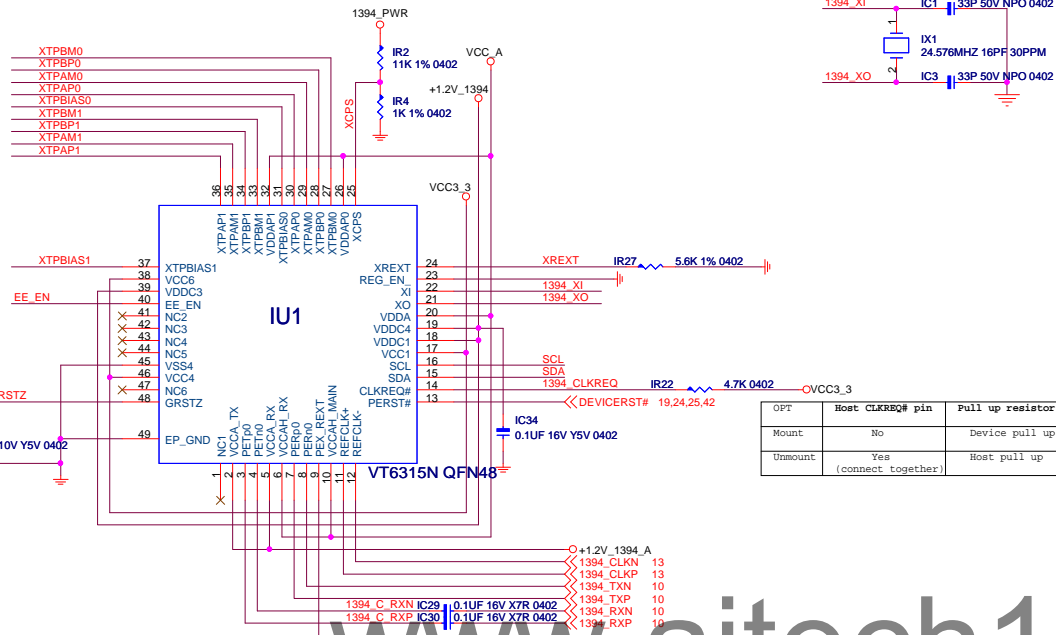
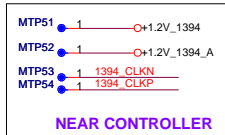




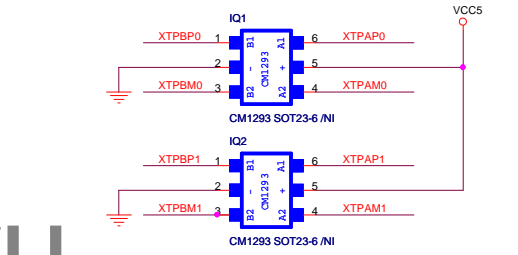
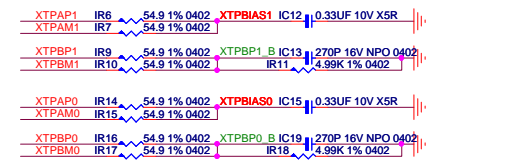




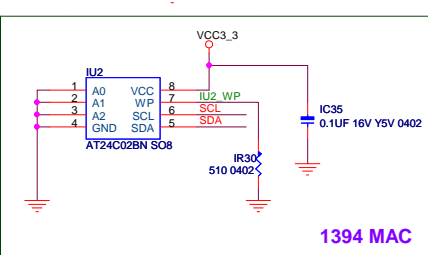
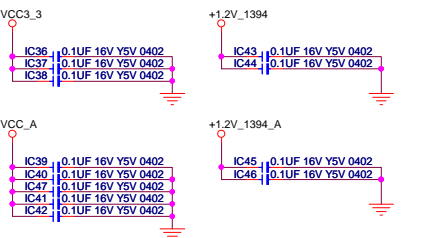
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PCIEX1 SLOT1 & 2 SLOT		
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FRONT 1394 JUMPER **REAR 1394 CONNECTOR**



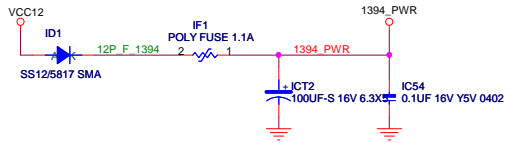
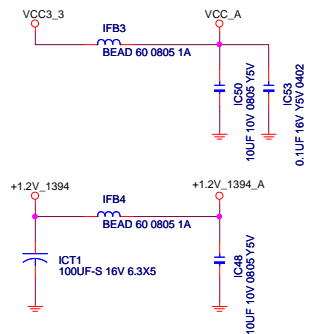
1394 CONNECTORS



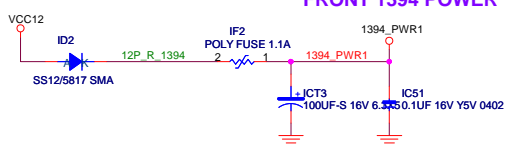
1394 MAC

If select shadow EEPROM,
please remove this part

Disable function	N/I
shadow EEPROM	STUFF



FRONT 1394 POWER



REAR 1394 POWER

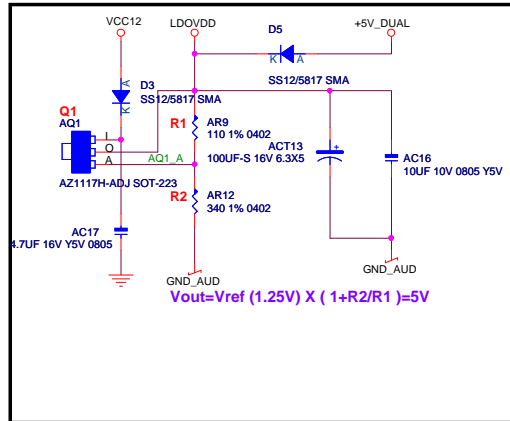
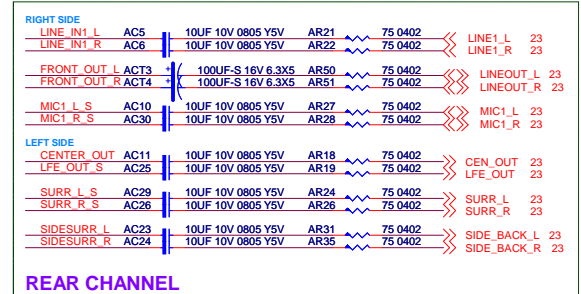
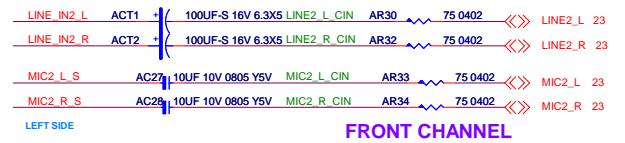
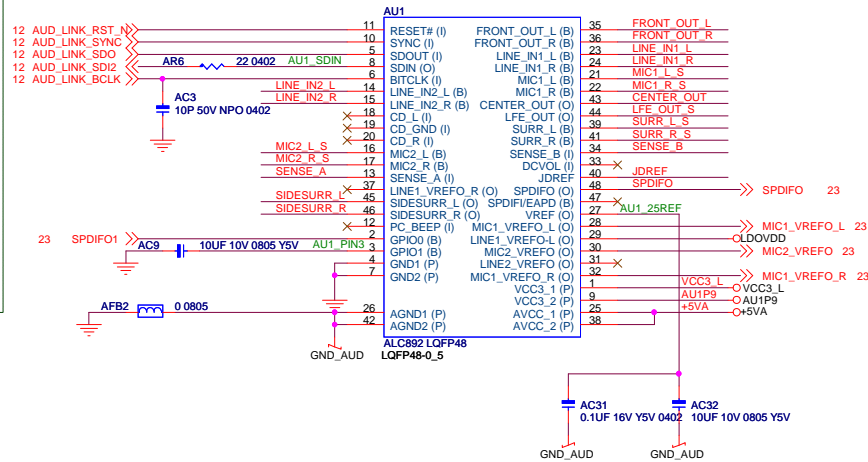
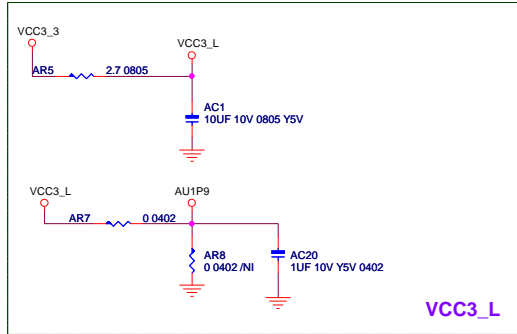
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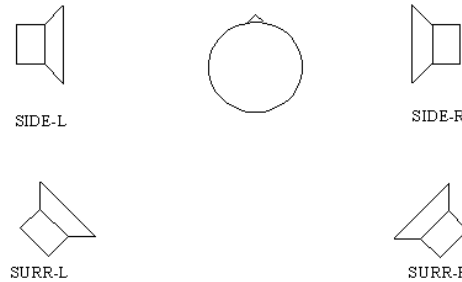
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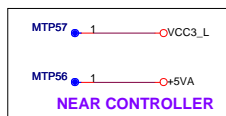
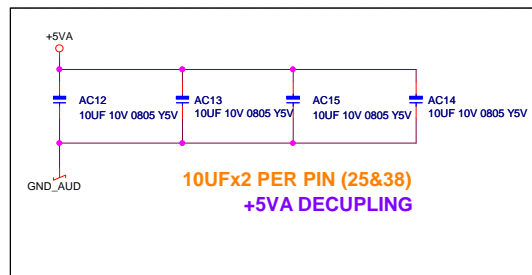
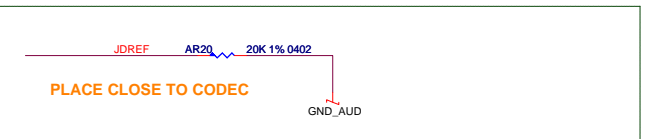
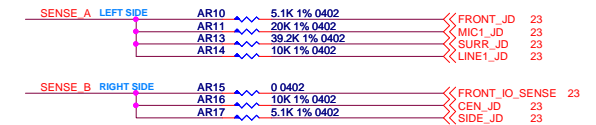
AUDIO PART: A+Reference



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CD IN CONNECTOR

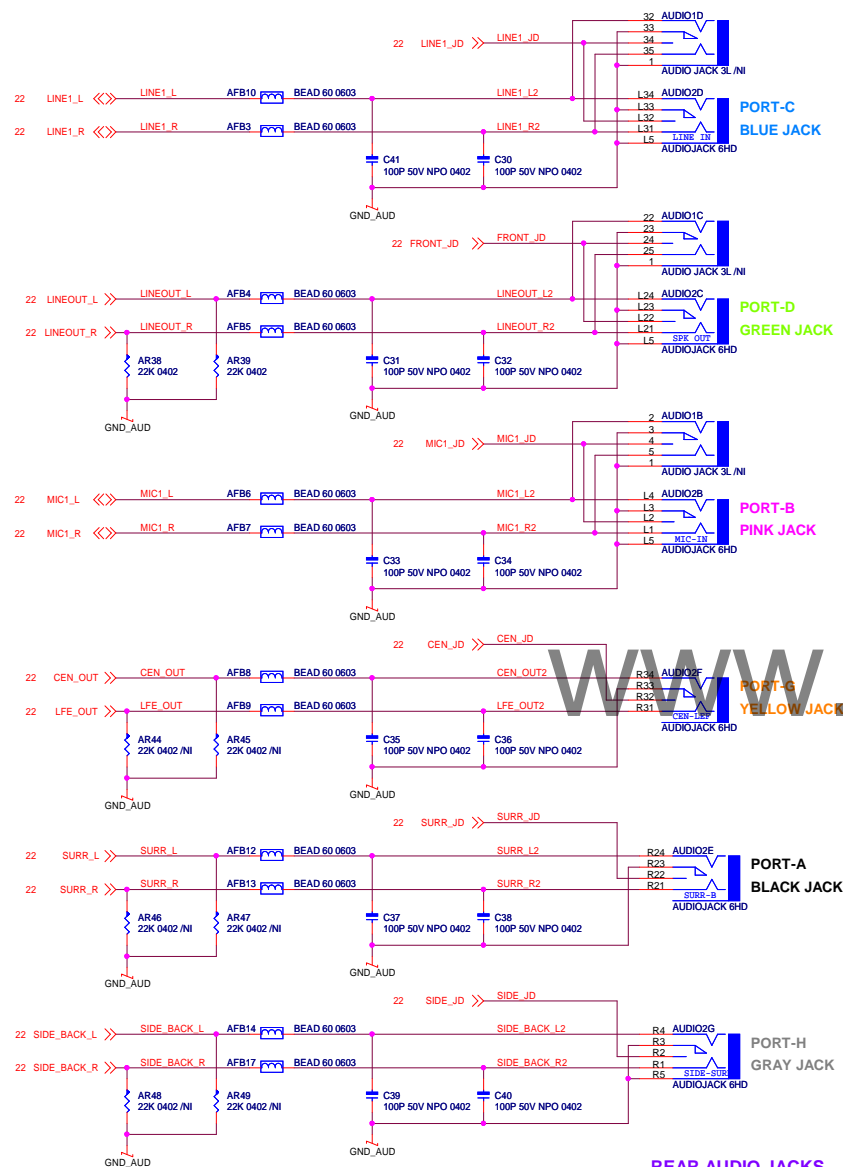


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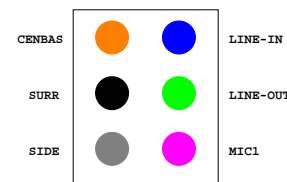
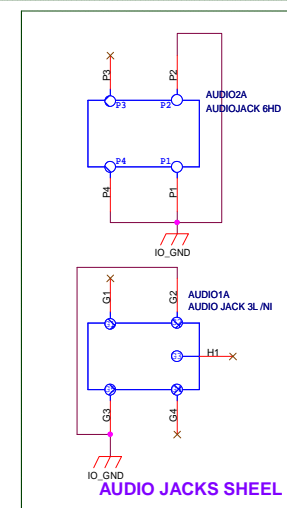
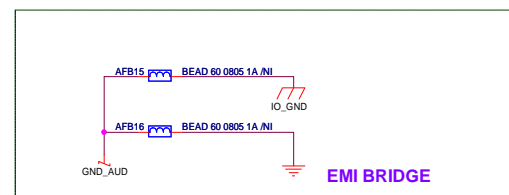
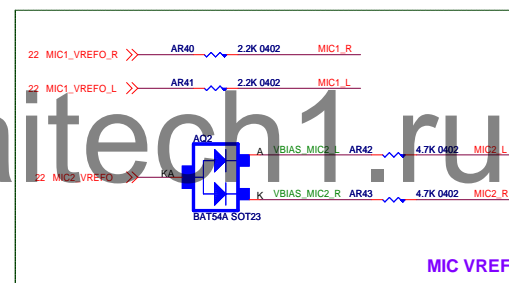
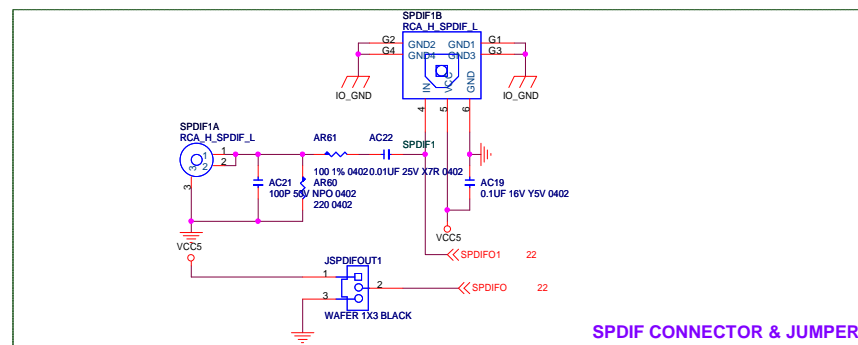
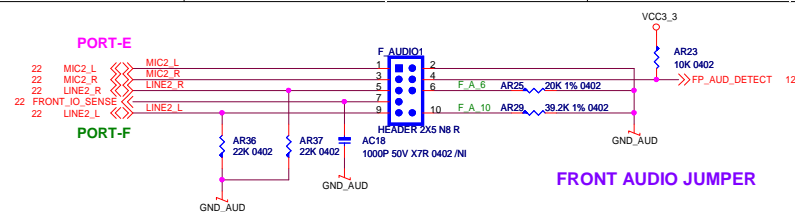
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REAR AUDIO JACKS



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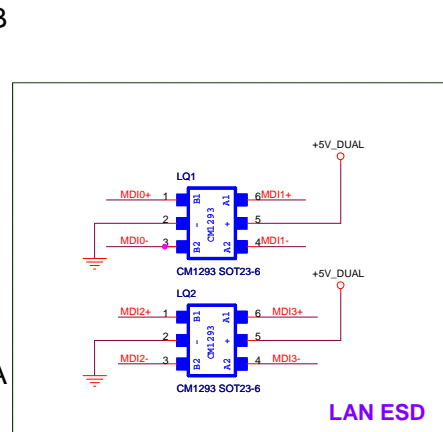
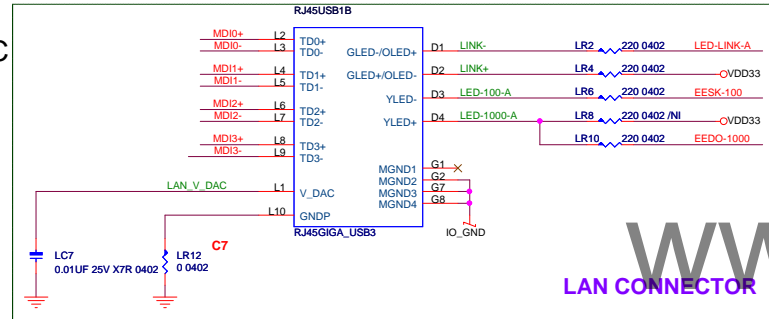
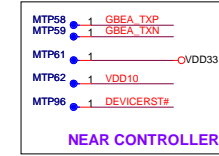
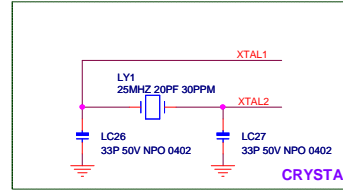
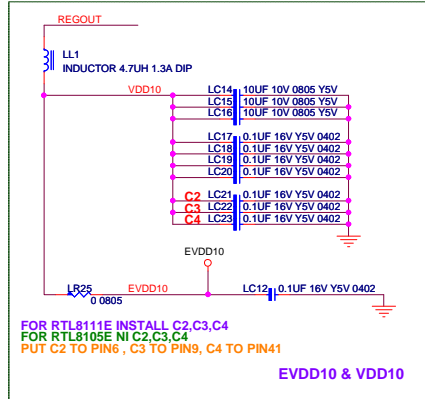
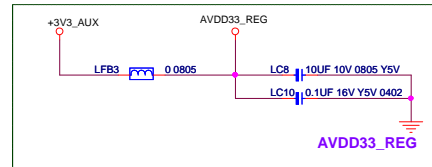
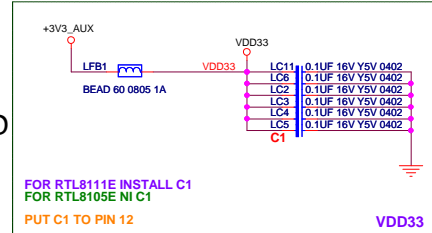
AUDIO CONNECTOR

IP67A-AHT

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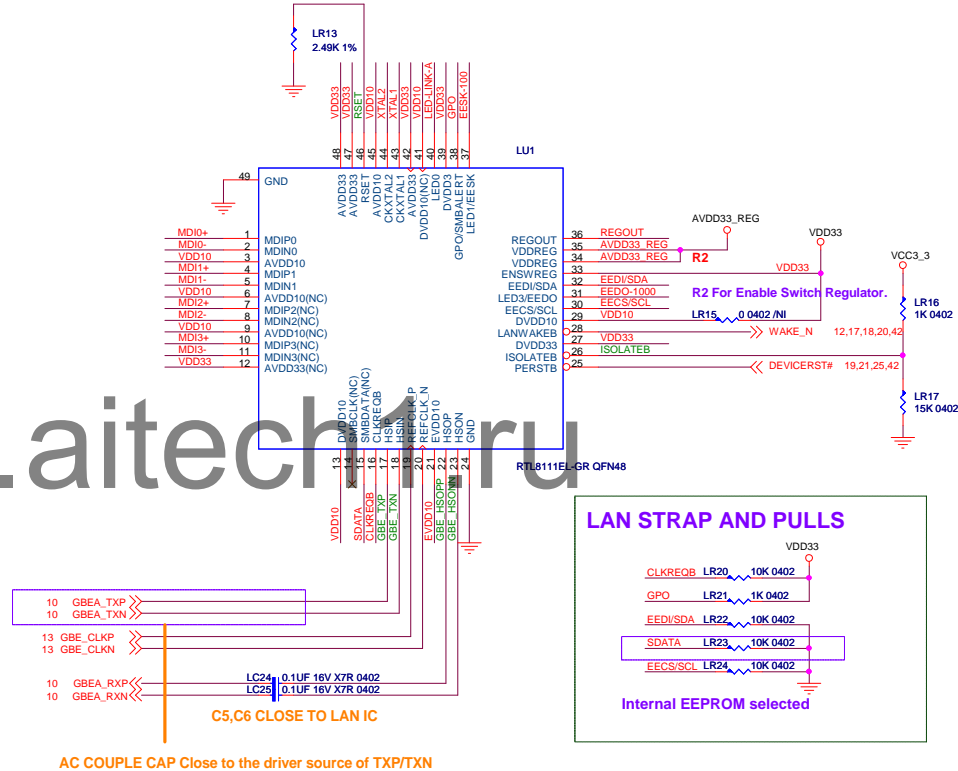
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LAN PART: L+Reference



COMPONENT CONTRAST LIST

LAN PARTS	C1	C2	C3	C4	C7	R1	R2	R3	R4	RJ45 CONN
RTL8111E	O	O	O	O	0ohm	X	X	O	O	LANUSB_GBMA
RTL8105E	X	X	X	X	0.1uF	O	O	X	X	RJ45USBA CONN



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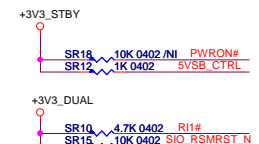
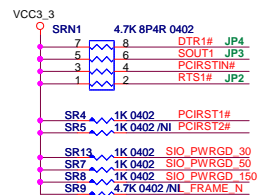
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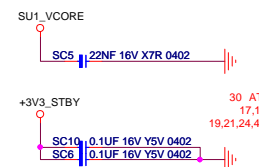
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SUPERIO PART: S+Reference

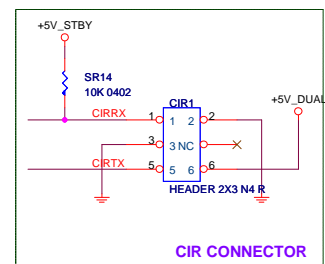
To PCH SMLINK BUS



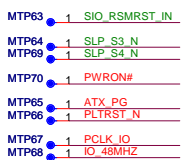
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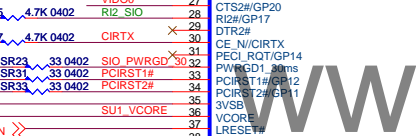
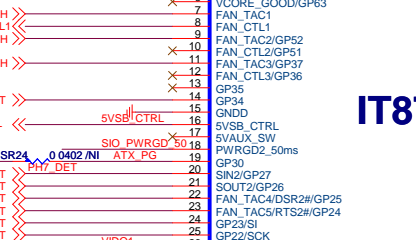
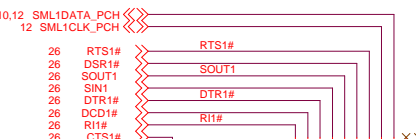
VCC CAPS



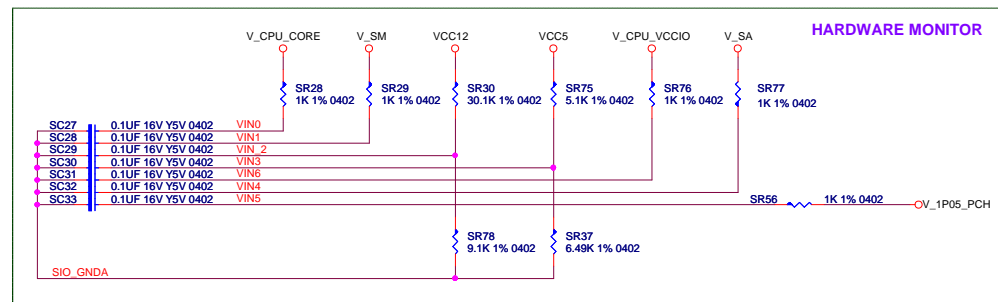
CIR CONNECTOR



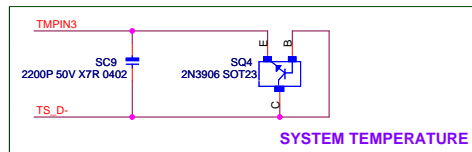
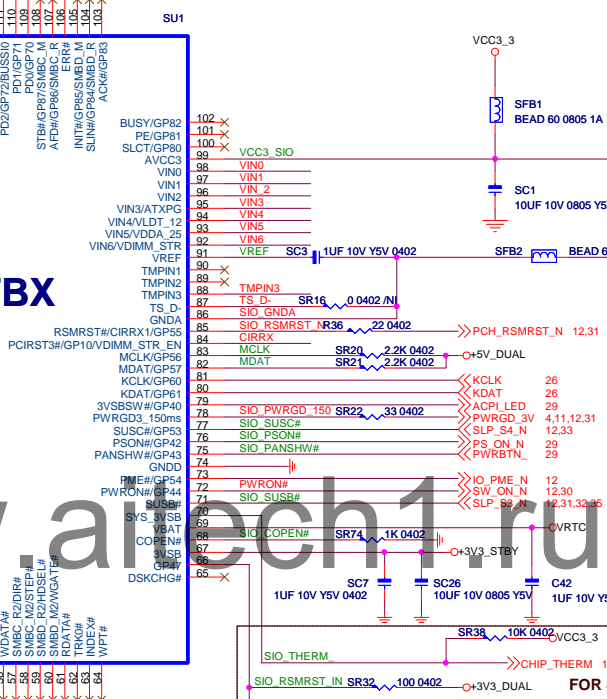
NEAR CONTROLLER



HARDWARE MONITOR

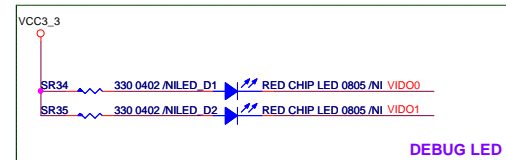
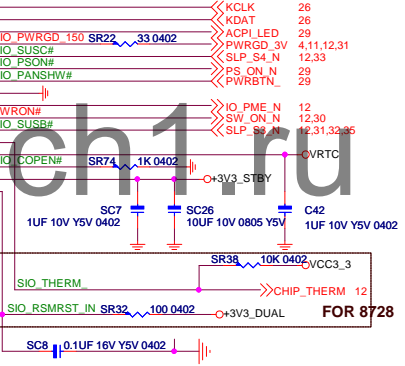
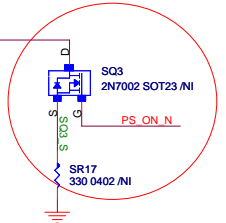


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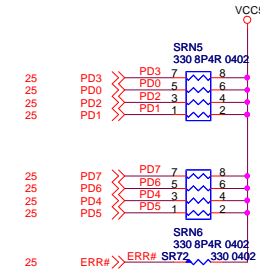
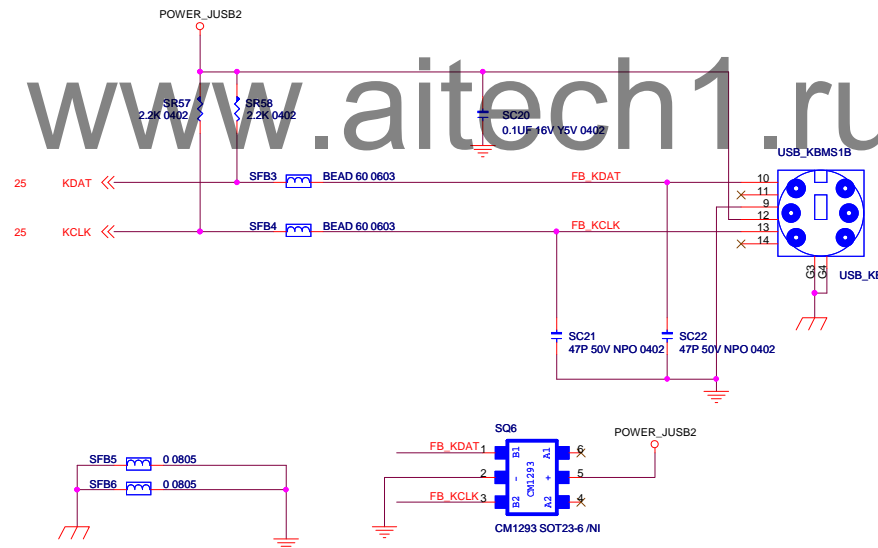
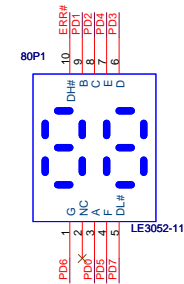
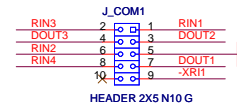
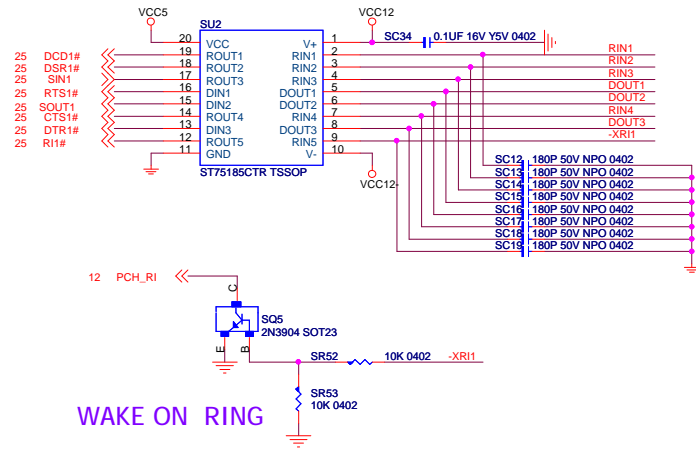
Reserved for NO phase detect use with WDT timer

4.29 WATCH_DOG << KR56 0.0402/NI PH7_DET



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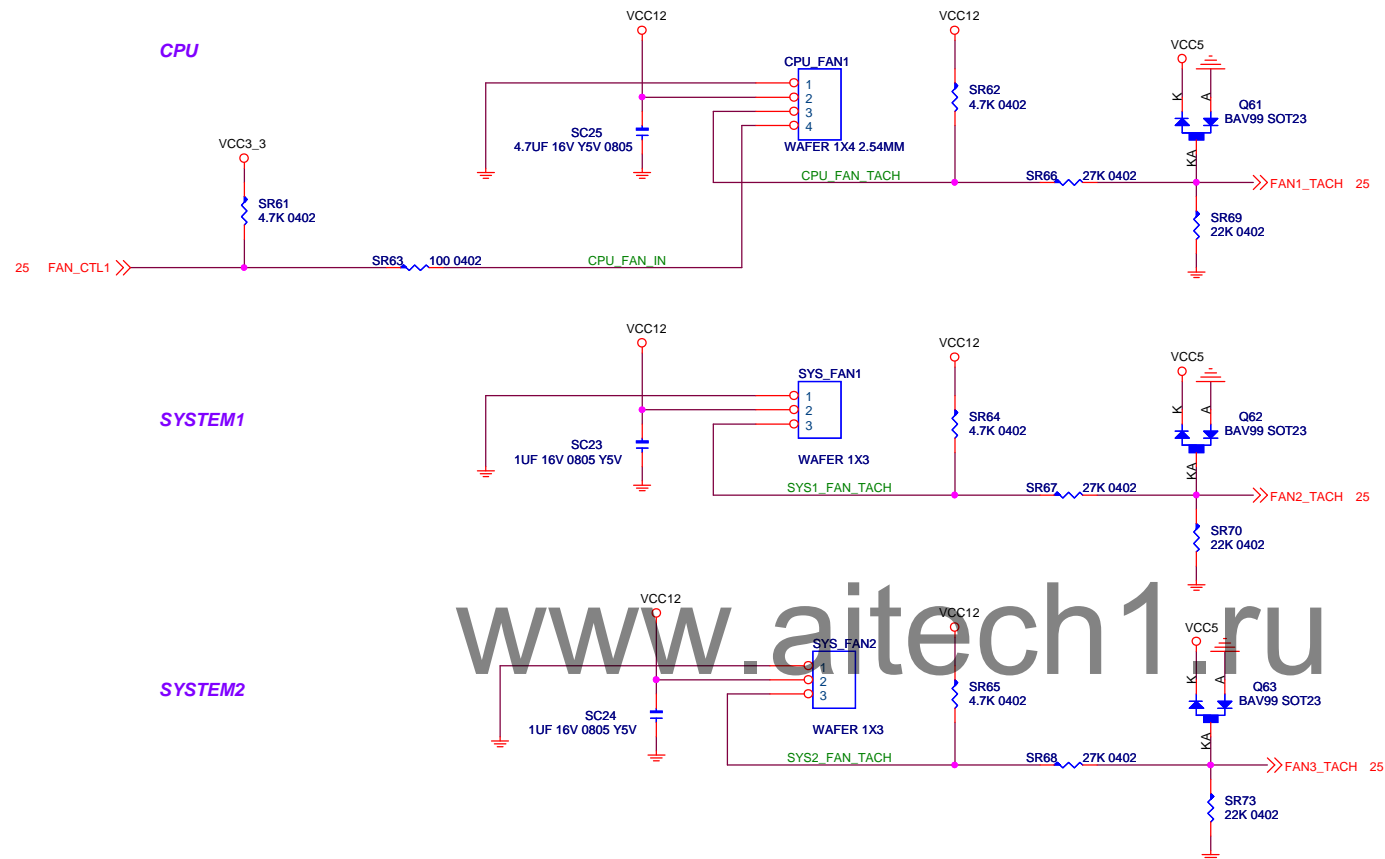



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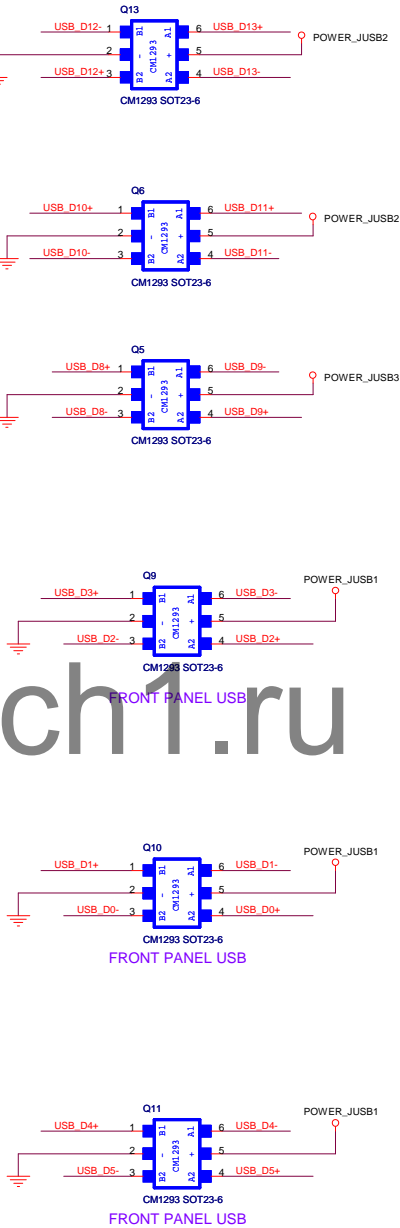
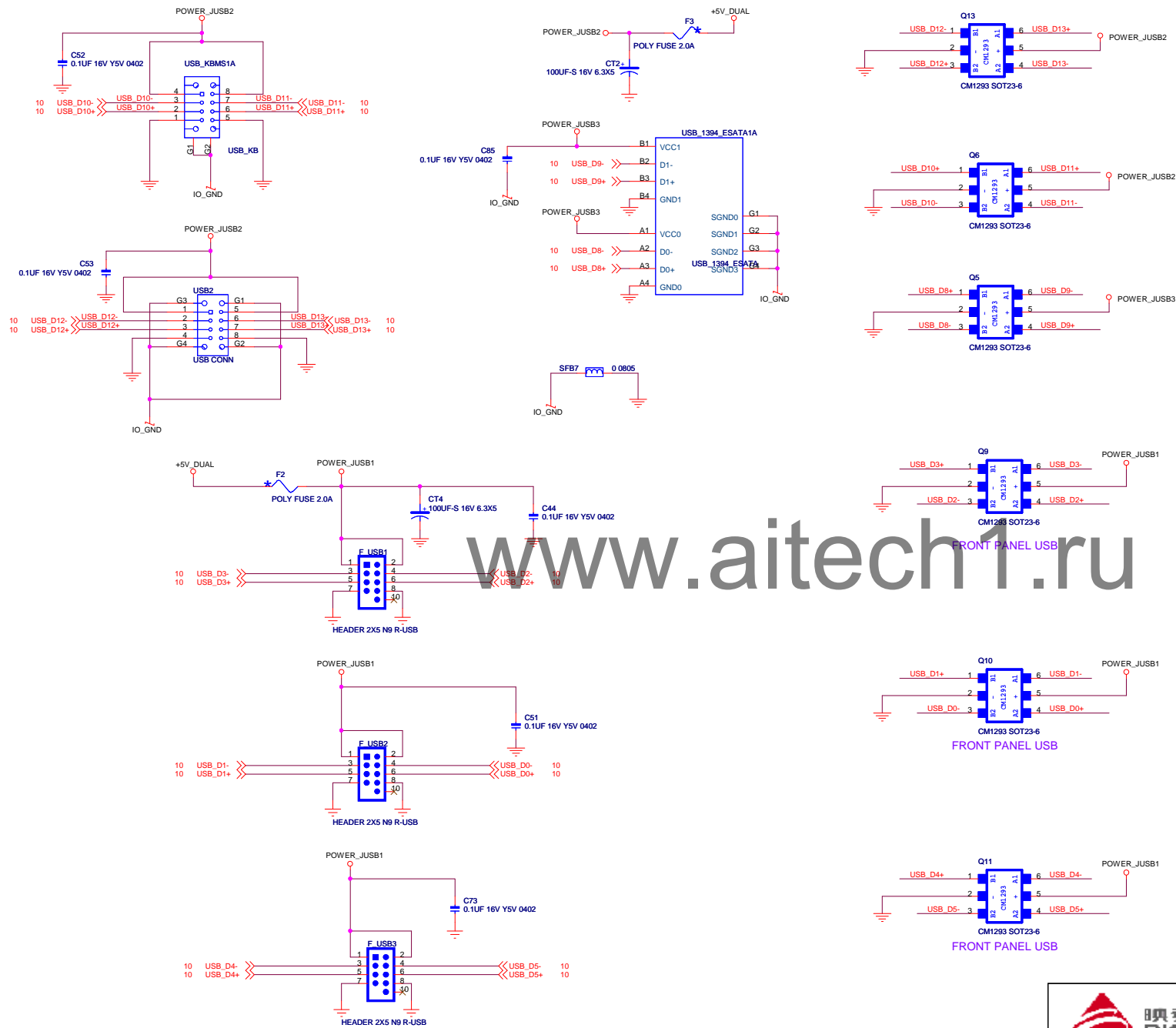
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Size: Custom Document Number: **IP67A-AHT** Rev: 5.0

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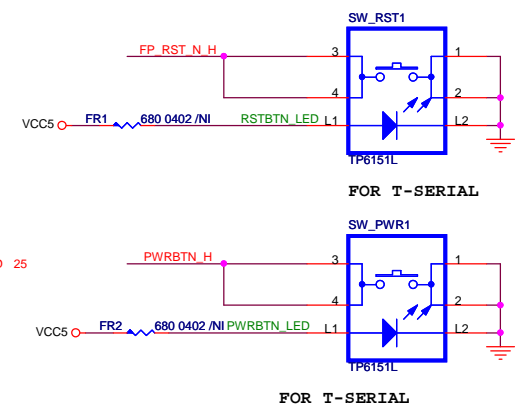
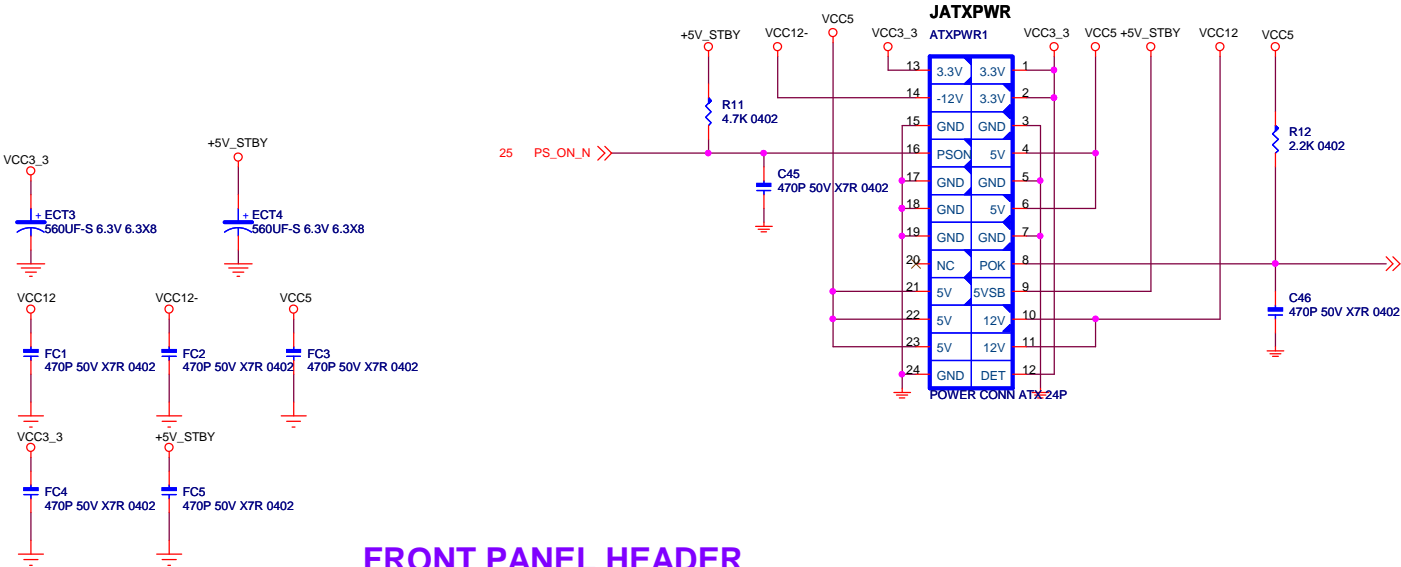
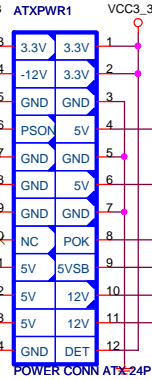


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Title HW MONITOR/FAN CONTROL		
Size Custom	Document Number IP67A-AHT	Rev 5.0
Date: Thursday, September 30, 2010 Sheet 27 of 43		

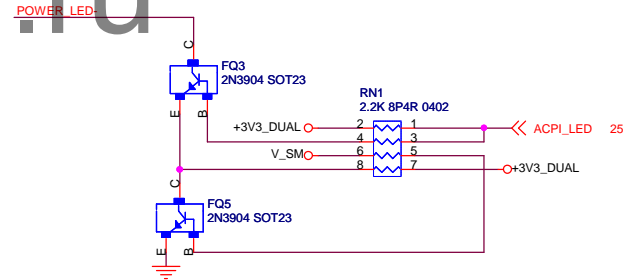
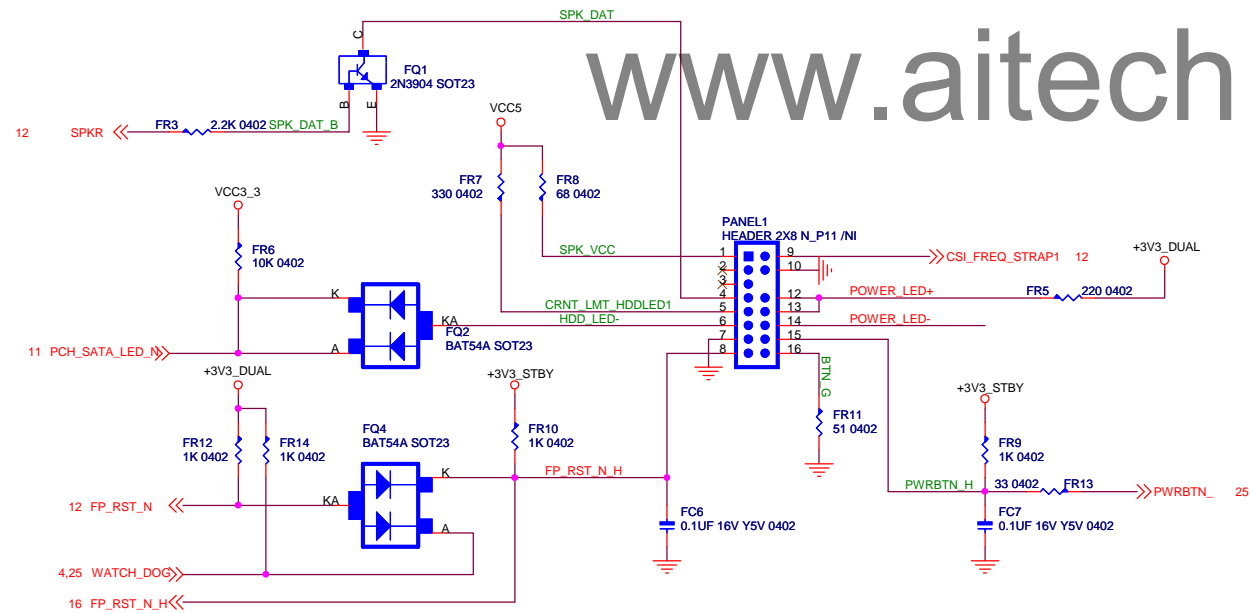


24 PIN POWER CONNECTOR

JATXPWR



FRONT PANEL HEADER

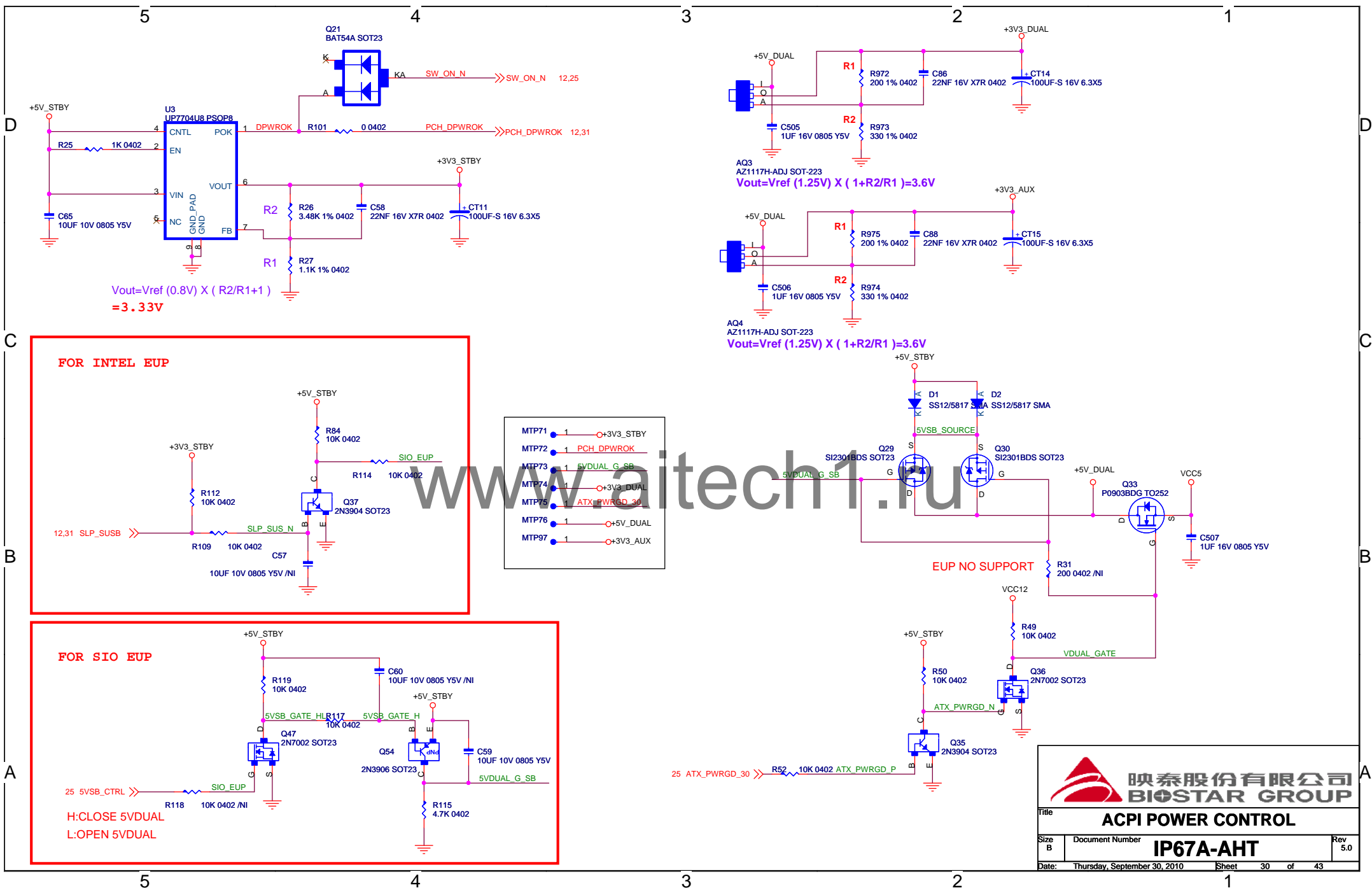


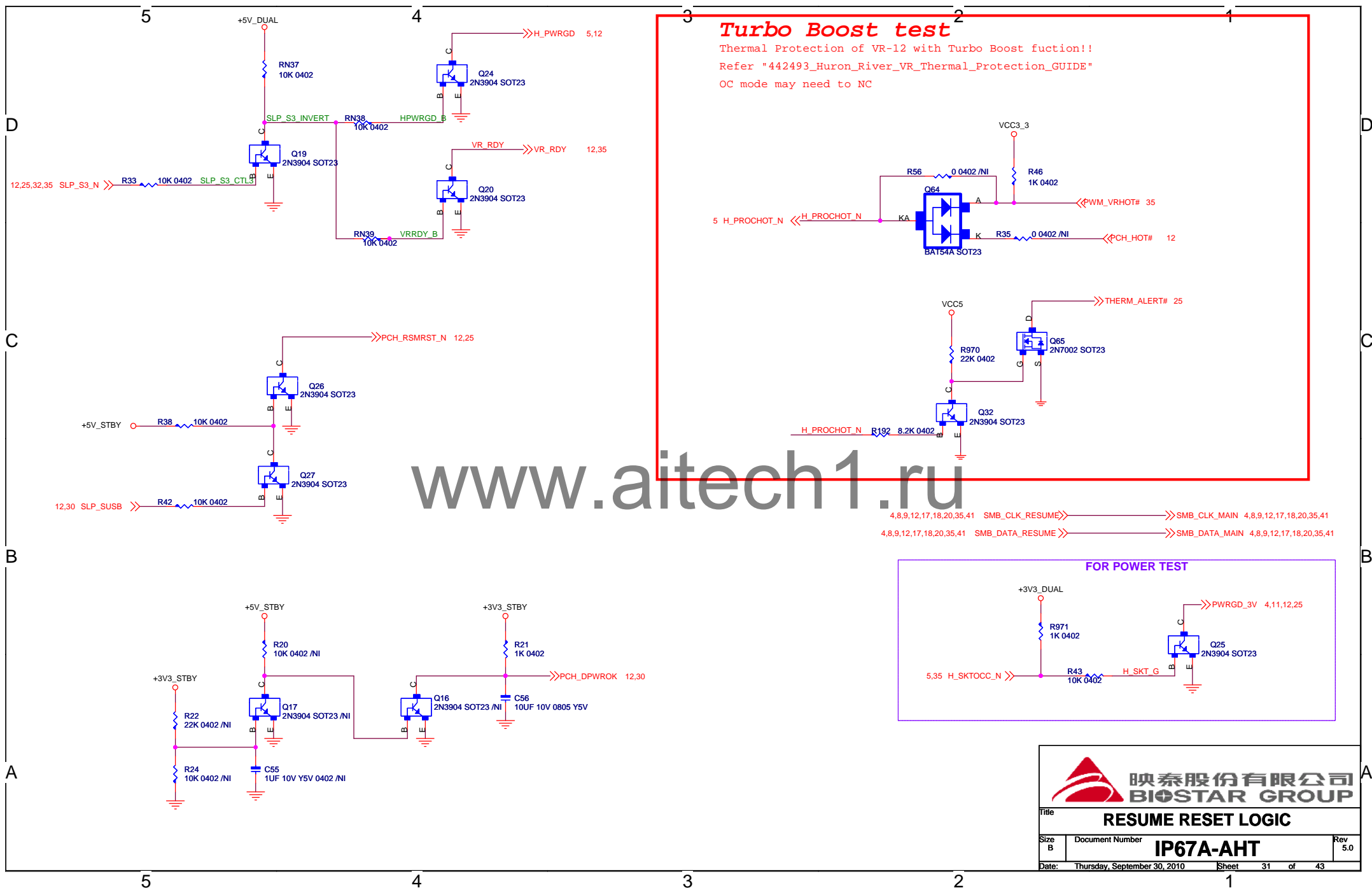
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BIOSTAR GROUP

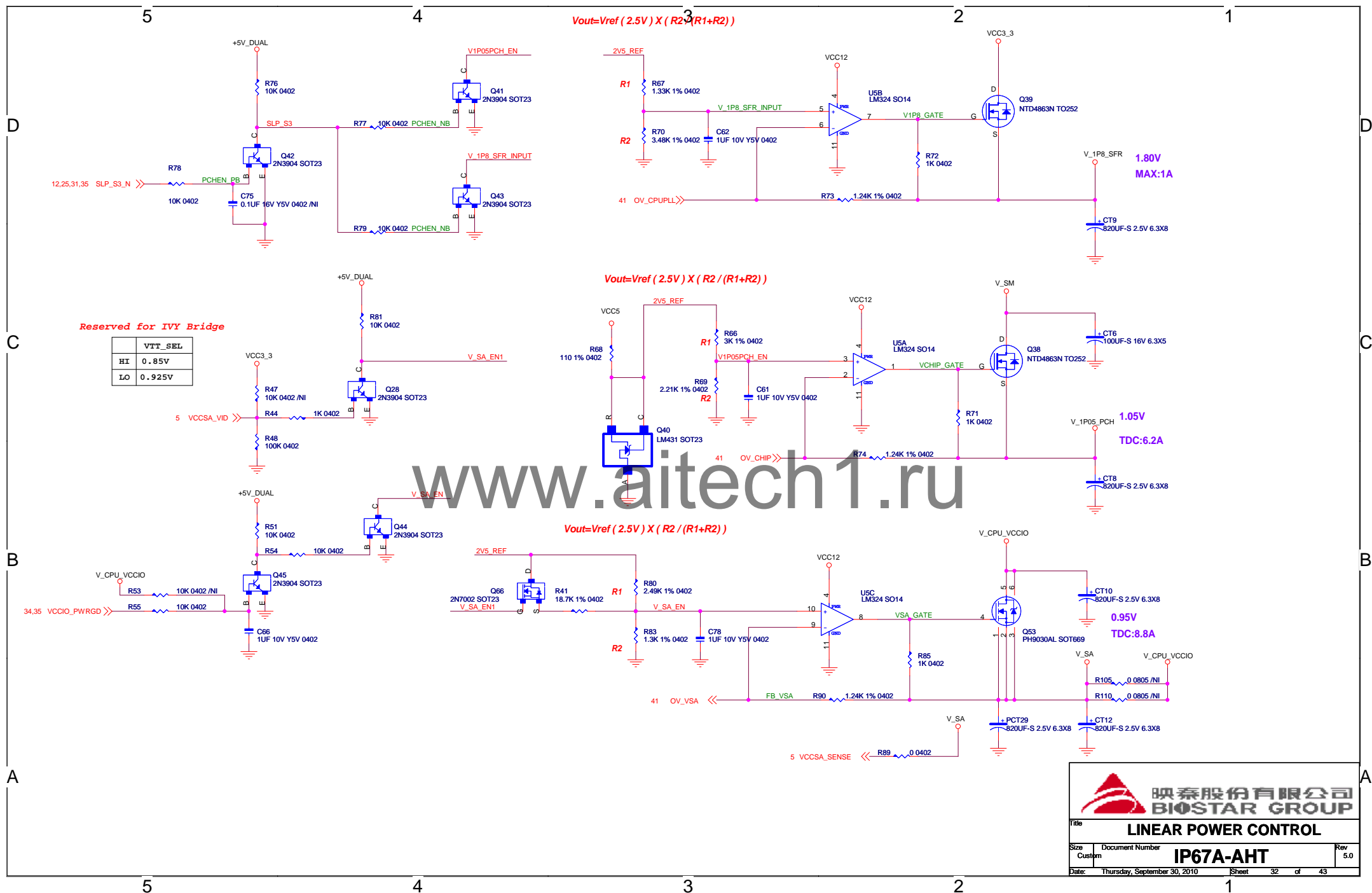
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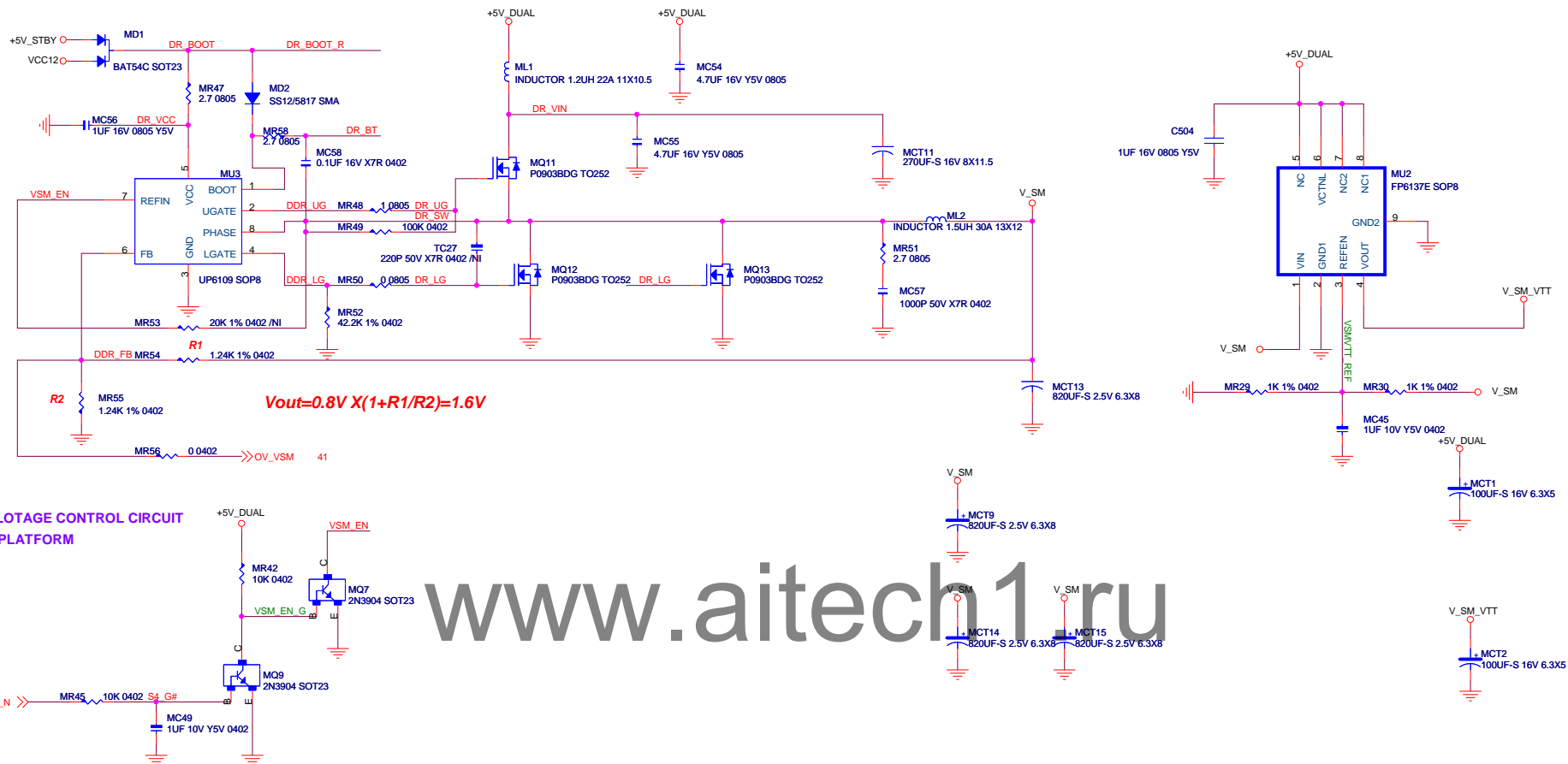
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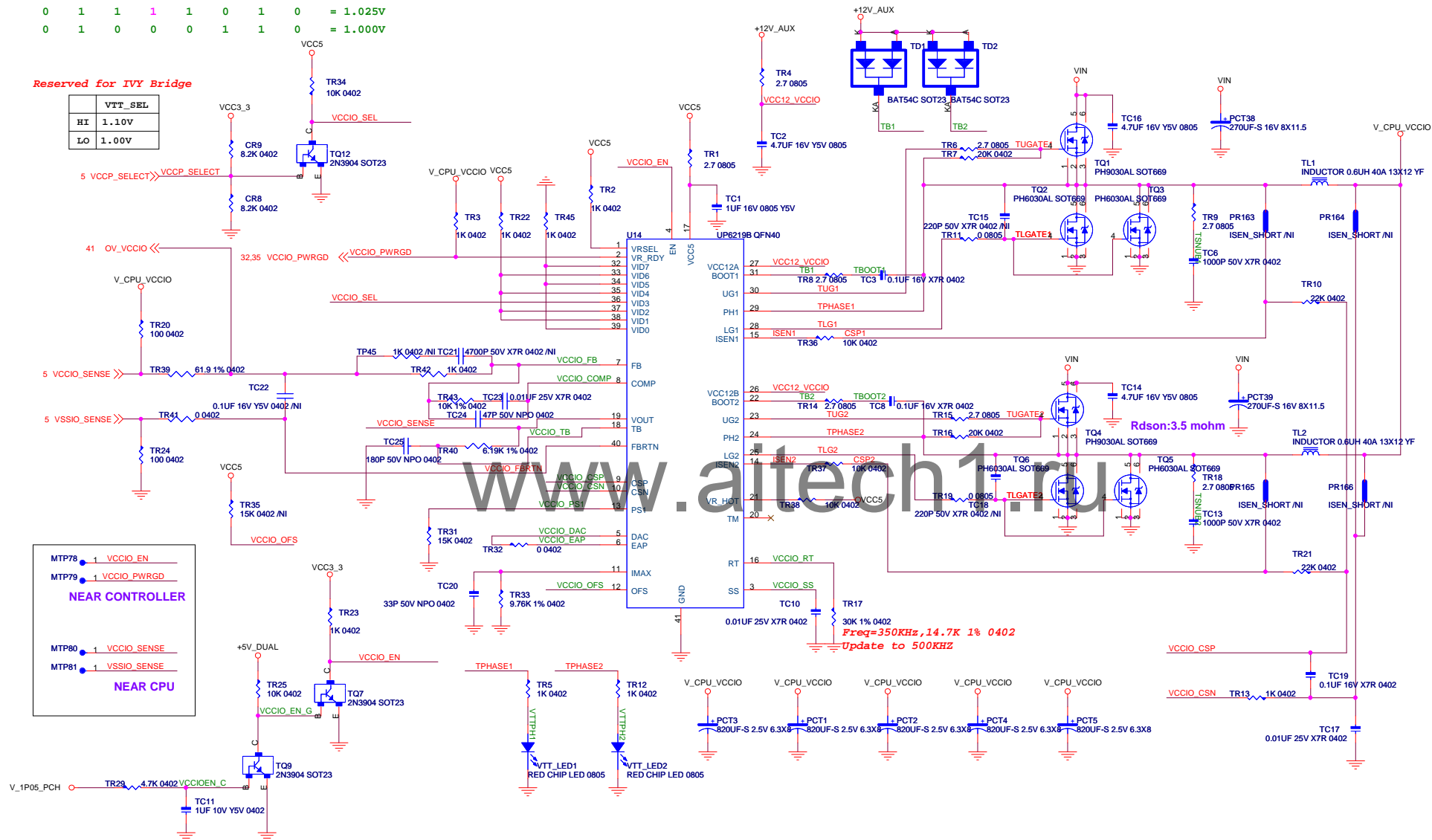
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 映泰股份有限公司 BIOSSTAR GROUP			
Title			
VSM DC-DC Conver			
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VID0	VID1	VID2	VID3	VID4	VID5	VID6	VID7	
0	1	1	0	1	0	1	0	= 1.075V
0	1	0	1	1	0	1	0	= 1.050V
0	1	1	1	1	0	1	0	= 1.025V
0	1	0	0	0	1	1	0	= 1.000V

Reserved for IVY Bridge

VTT_SEL	
HI	1.10V
LO	1.00V

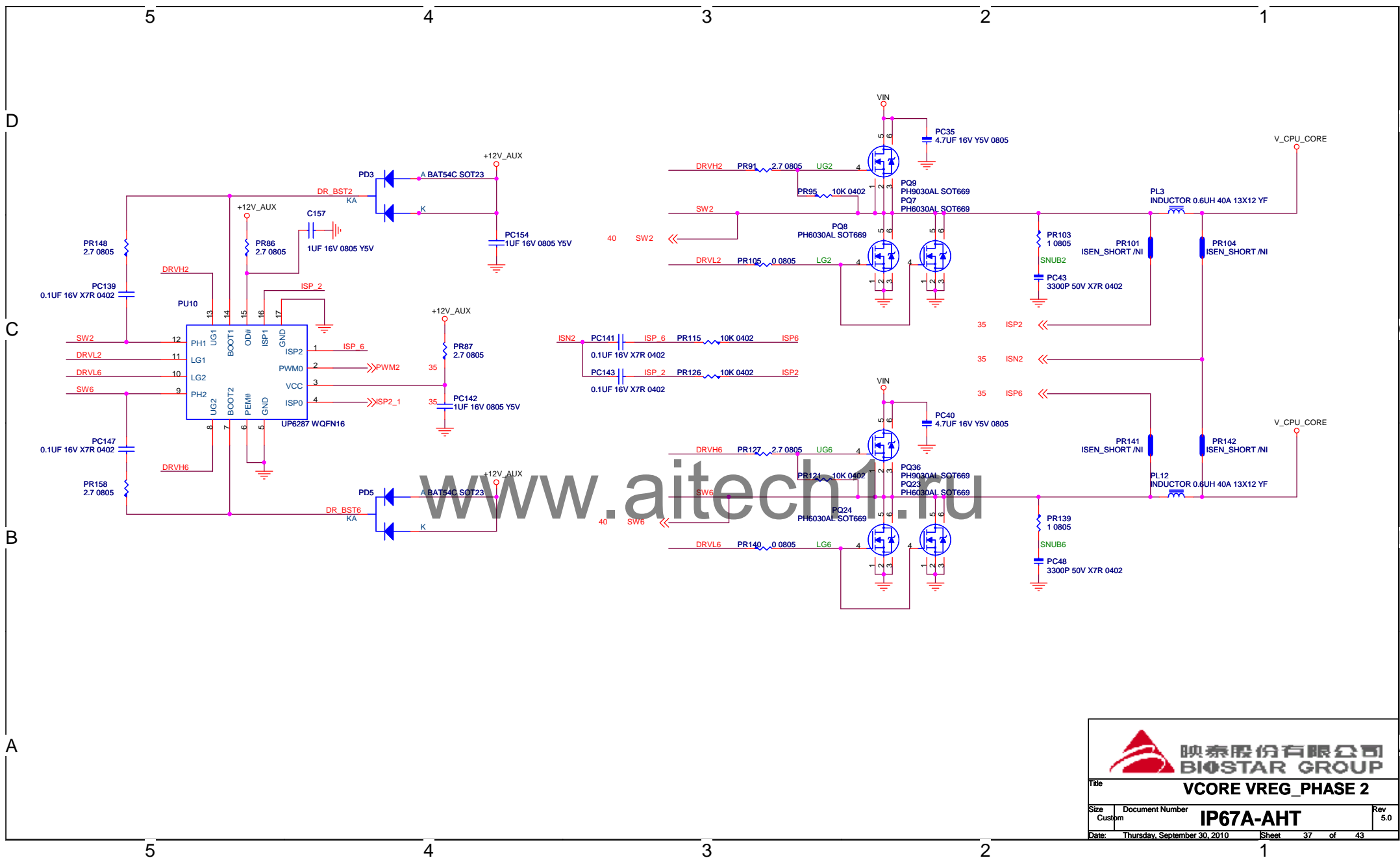





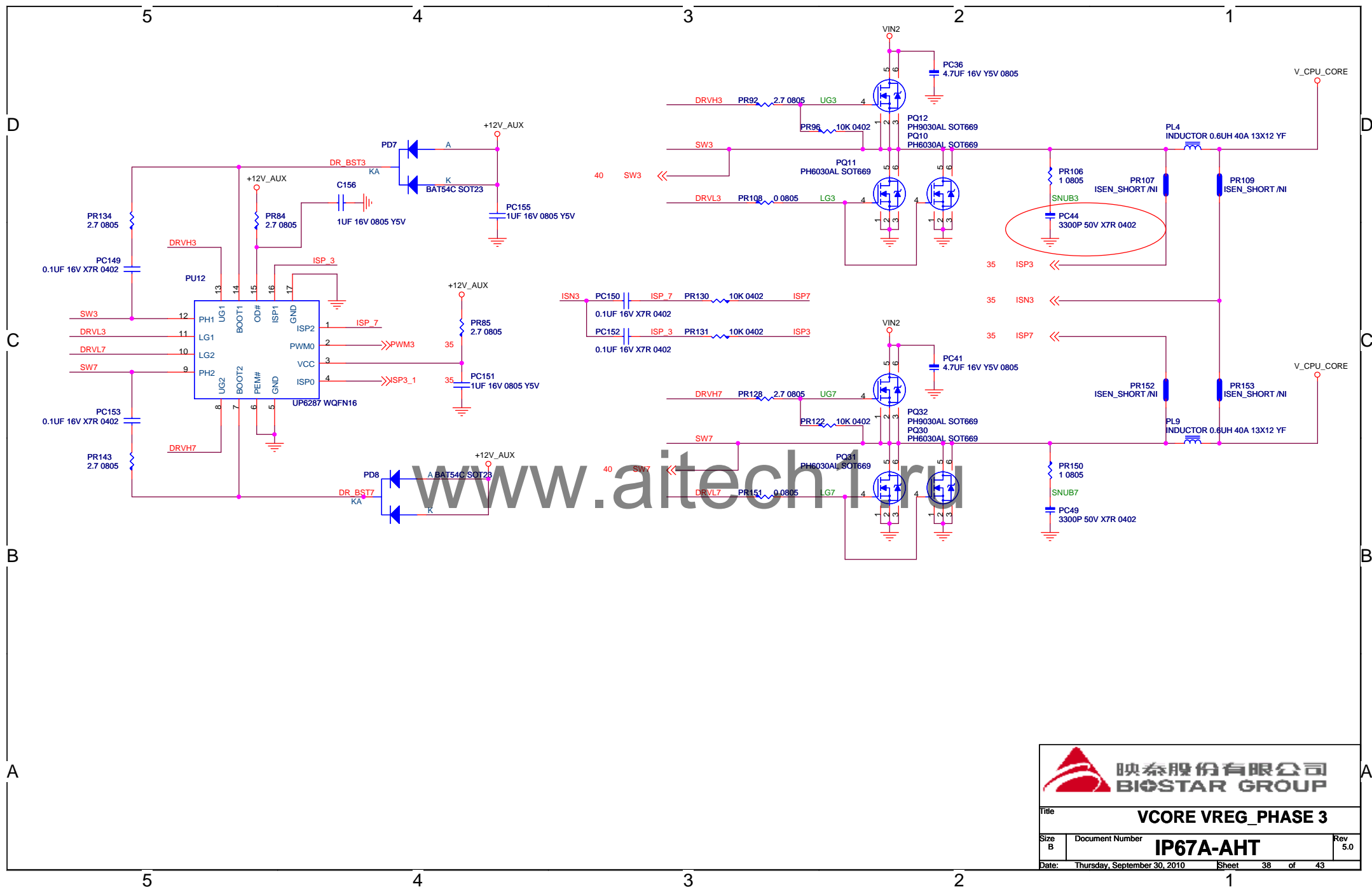
映泰股份有限公司
BIOSAR GROUP

Title: VTT DC-DC Converter		
Size: Custom	Document Number: IP67A-AHT	Rev: 5.0
Date: Thursday, September 30, 2010	Sheet: 34	of 43

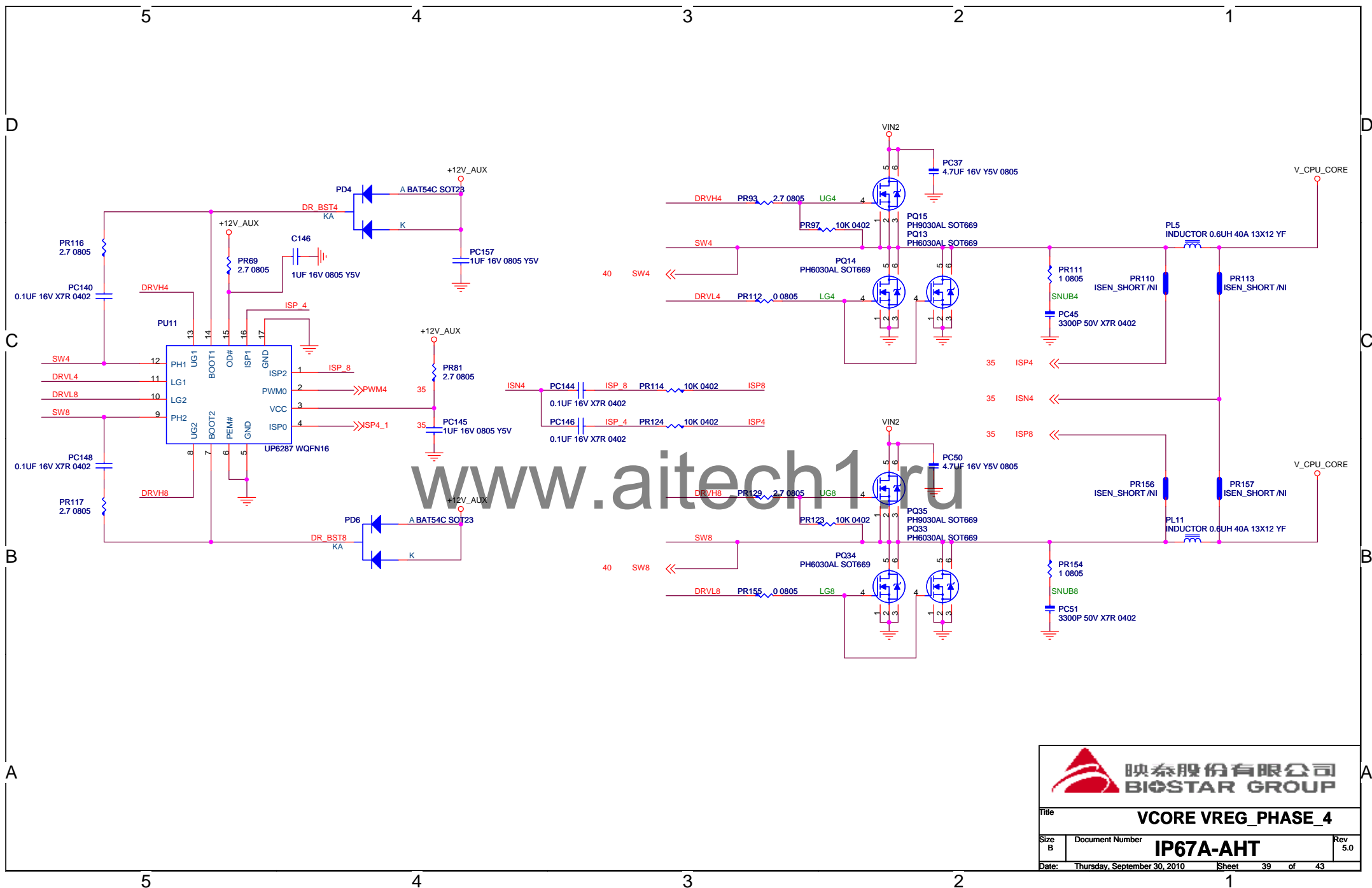


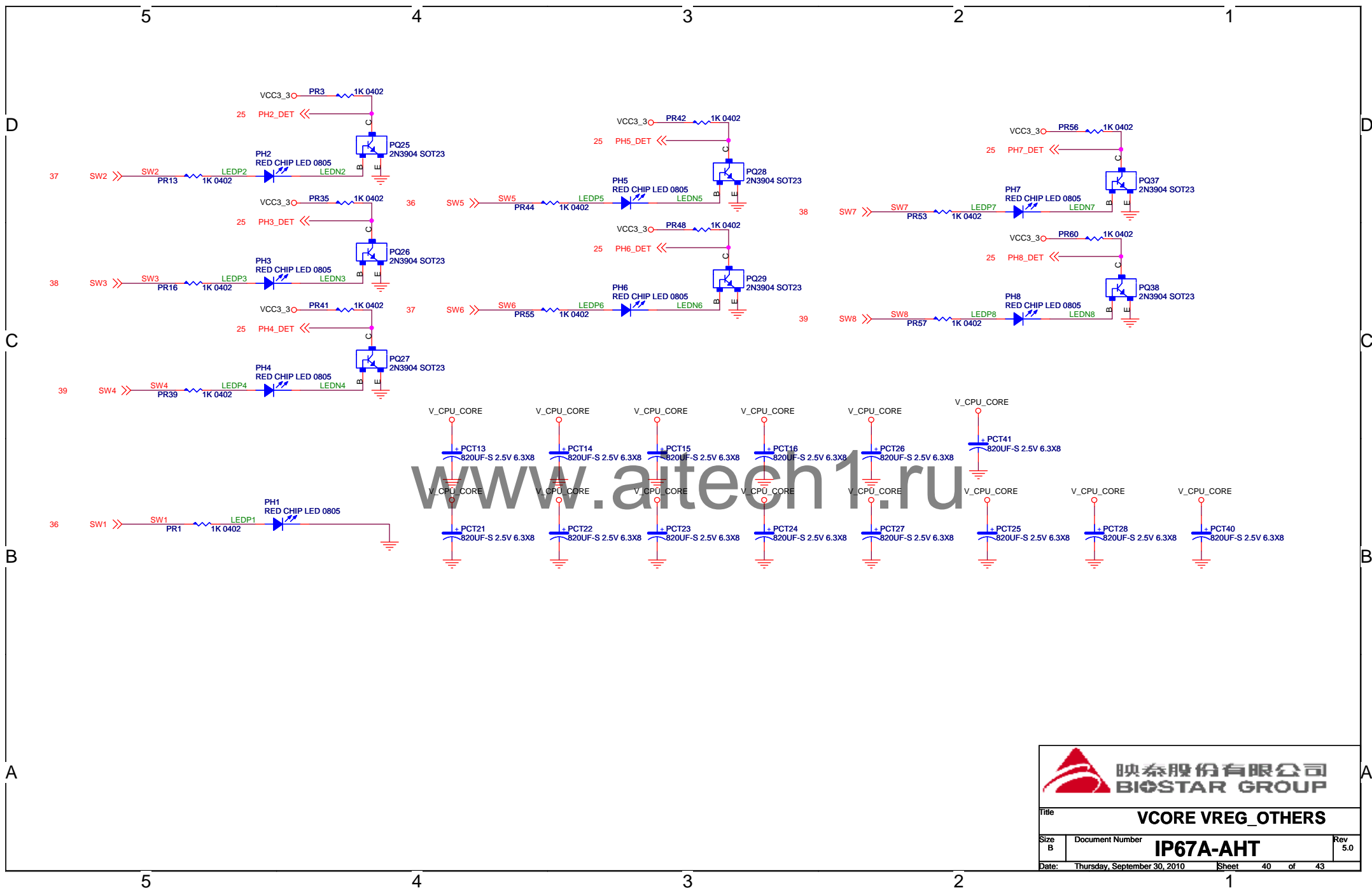


 映泰股份有限公司 BIOSTAR GROUP			
Title VCORE VREG_PHASE 2			
Size Custom	Document Number IP67A-AHT		Rev 5.0
Date: Thursday, September 30, 2010	Sheet	37	of 43

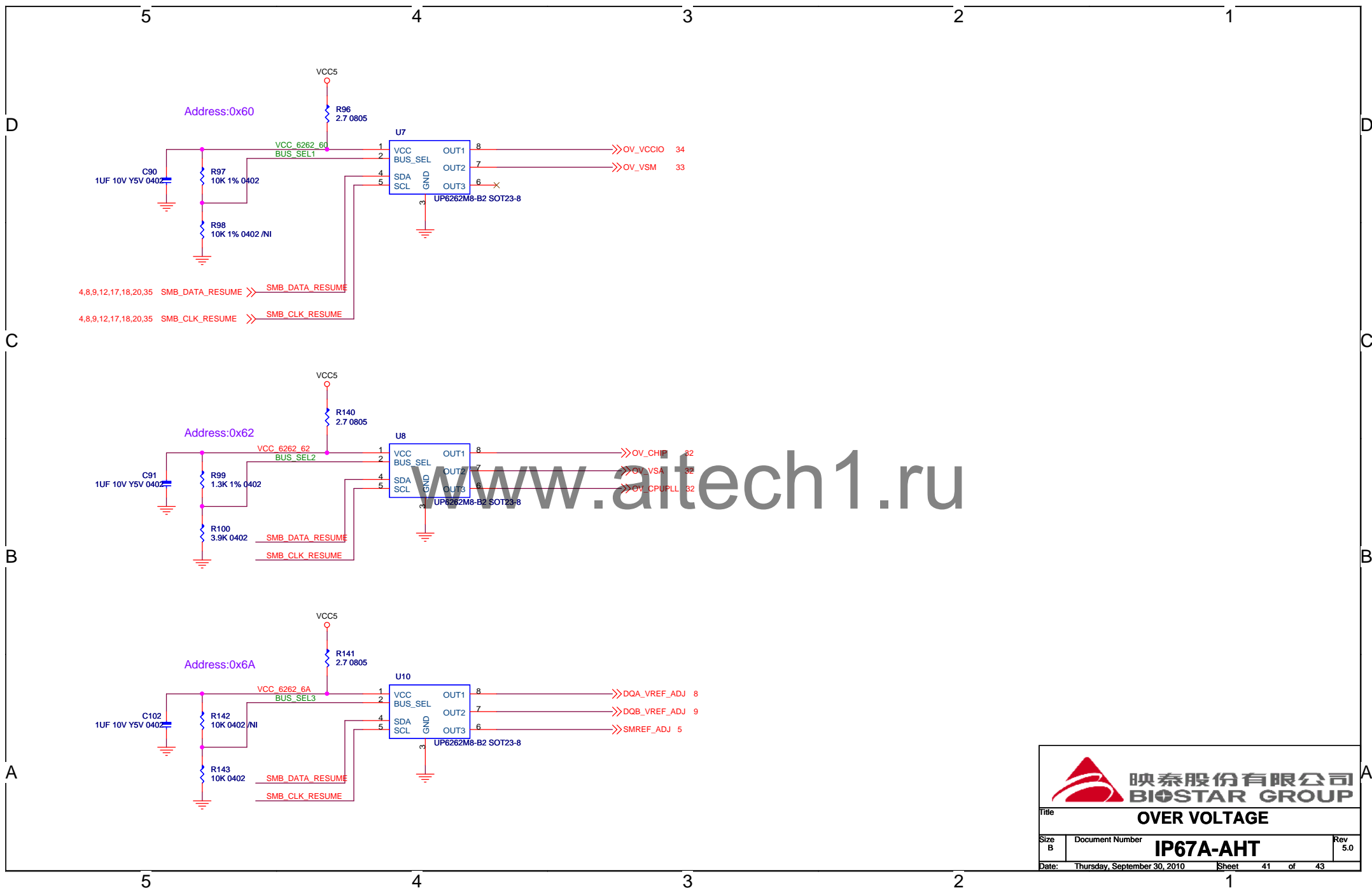



 映泰股份有限公司 BIOSSTAR GROUP			
Title VCORE VREG_PHASE 3			
Size B	Document Number IP67A-AHT		Rev 5.0
Date: Thursday, September 30, 2010	Sheet 38	of 43	1



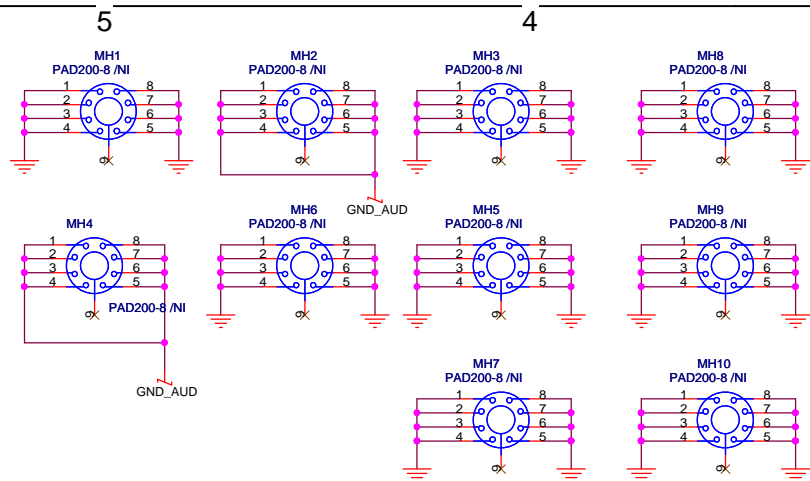


 映泰股份有限公司 BIOSSTAR GROUP			
Title VCORE VREG_OTHERS			
Size B	Document Number IP67A-AHT		Rev 5.0
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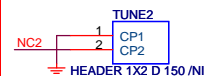
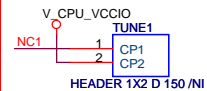
 映泰股份有限公司 BIOSSTAR GROUP			
Title			
OVER VOLTAGE			
Size B	Document Number		Rev
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double check POOL Structures !!

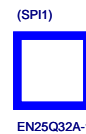
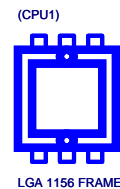
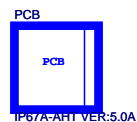
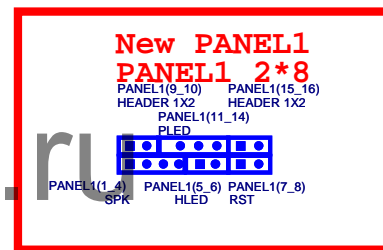
Impedance Testing Coupon



Traces Typical Zo

Data 40 ohm
CMD/ADDR 32 ohm
CLK 62 ohm

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Title BOM			
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